European Core Technologies
for future connectivity systems and components

Call/Topic: H2020 ICT-42-2020

Grant Agreement Number: 956830

Deliverable

D3.4 Intermediate COREnect industry roadmap

Deliverable type:	Report
WP number and title:	WP3 (Roadmap and recommendations)
Dissemination level:	Public
Due date:	31.01.2022
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Document History

Version	Date	Author/Editor	Description
0.1	11.10.2021	IMEC	Outline
0.2	15.12.2021	All involved partners with support of experts	Completing most sections
0.3	17.12.2021	All involved partners with support of experts	All sections completed
0.4	17.12.2021	IMEC	Formatted and cleaned
0.5	04.01.2022	Internal reviewers	Feedback and corrections applied
0.6	10.01.2022	Experts and consortium partner	Feedback implemented
1.0	14.01.2022	IMEC	Final version

List of Abbreviations

Abbreviation	Denotation
4G	4th generation mobile communication
5G	5th generation mobile communication
5G-ACIA	5G alliance for connected industries and automation
6G	6th generation mobile communication
AAU	Active antenna unit
ADAS	Advanced Driver Assistance Systems
ADC	Analog to digital converter
AI	Artificial Intelligence
API	Application programming interface
ARM	Advanced RISC machine
ASIC	Application-specific integrated circuit
BAW	Bulk acoustic wave
BiCMOS	Bipolar CMOS
BT	Bluetooth
CAPEX	Capital expenditures
CAPI	Common ISDN application programming interface
CCIX	Cache coherent interconnect
CMOS	Complementary metal oxide semiconductor
COVID	Coronavirus pandemic
CPO	Co-Packaged Optics
CPU	Central processing unit
CU	Central unit
CXL	Compute express link
DAC	Digital to analog converter
DBT	Dynamic binary translation
DBT	Dynamic binary translation
DC	Data center
DDR	Double data rate
DeMUX	Demultiplexer
DIMM	Dual in-line memory module
DPU	Data processing unit
DSL	Domain-specific language
DSP	Digital signal processing

Abbreviation	Denotation
IP	Intellectual property
IPR	Intellectual property rights
ISA	Instruction set architecture
ISG	Industry specification group
IWD	Intelligent wearable devices
JEDEC	Joint electron device engineering council
KPI	Key performance indicator
LDMOS	Planar double diffused MOSFET
LNA	Low noise amplifier
MCM	Multi-chip modules
MCU	Microcontroller unit
MEMS	Micro-electro-mechanical systems
MIIT	Ministry of industry and information technology (China)
MIMO	Multiple input multiple output
ML	Machine learning
MLC	Multi-level cell
MPSOC	Multiprocessor system on a chip
MRAM	Magneto resistive random-access memory
mURLLC	massive URLLC
MUX	Multiplexer
NB-IoT	Narrowband IoT
NIC	Network interface card
NVM	Non-volatile memory
O/E	Optical-to-electronics
OEM	Original equipment manufacturer
OS	Operating system
OTA	Over the air
PA	Power amplifier
PC	Personal computer
PCB	Printed circuit board
PCI-SIG	Peripheral component interconnect special interest group
PCM	Phase-change memory
PCP	Programmable computing platforms

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DU	Distributed unit
E/O	Electronics-to-optical
ECS	Electronic circuits and systems
ECU	Electronic control unit
EDA	Electronic design automation
eDRAM	Embedded dynamic random-access memory
EG	Expert group
EIRP	Effective isotopically radiated power
eMR	Electronic medical record
eNVM	Embedded non-volatile memory
FBAR	Film bulk acoustic resonator
FDSOI	Fully depleted silicon on insulator
FeRAM	Ferroelectric random-access memory
FinFET	Fin field-effect transistor
FPGA	Field programmable gate array
FTTH	Fiber to the home
FW	Firmware
GaN	Gallium nitride
GDPR	General data protection regulation
GPU	Graphical processing unit
h-BN	Hexagonal boron nitride
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility transistor
HMI	Human-machine interface
HPC	High performance computing
HW	Hardware
I/O	Input /output
IC	Integrated circuit
IDM	Integrated device manufacturer
IIoT	Industrial internet of things
InP	Indium phosphide
IoT	Internet of things

PON	Passive optical network
PUF	Physical unclonable function
QoS	Quality of service
R&I	Research and innovation
RADCOM	Radar and Communication
RAN	Radio access network
RF	Radio frequency
RFID	Radio-frequency identification
RISC	Reduced instruction set computer
ROW	Rest of the world
RTN	Random telegraph noise
RTO	Research and Technology Organization
RU	Radio unit
SAW	Surface acoustic wave
SiGe	Silicon germanium
SiP	Systems-in-package
SME	Small and medium-sized enterprise
SoC	System on chip
SOI	Silicon on insulator
SRAM	Static random-access memory
SW	Software
SWOT	Strengths weaknesses opportunities threats
TRL	Technology readiness level
TSN	Time-sensitive networking
TSV	Through silicon via
UE	User Equipment
UI	User interface
URLLC	Ultra-reliable low latency communications
USA	United States of America
UV	Ultraviolet lithography
UWB	Ultra-wideband
V2V	Vehicle to vehicle
V2X	Vehicle to everything

Disclaimer

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1. Introduction

One of the key COREnect objectives is to define a strategic R&I roadmap for future European connectivity systems and components, supporting Europe's strategic autonomy and sovereignty objectives. This roadmap is being defined based on input from all relevant stakeholders across different domains and communities (including SNS and KDT), covering the relevant actors from industry, research, academia, associations, policy analysis etc.

An end-to-end view of future connectivity systems is depicted in Figure 1. To achieve the upcoming needs from emerging applications in e.g., industrial automation, such connectivity systems need to offer extreme high capacity, extreme coverage, extreme low latency and high reliability, all at low energy and cost.

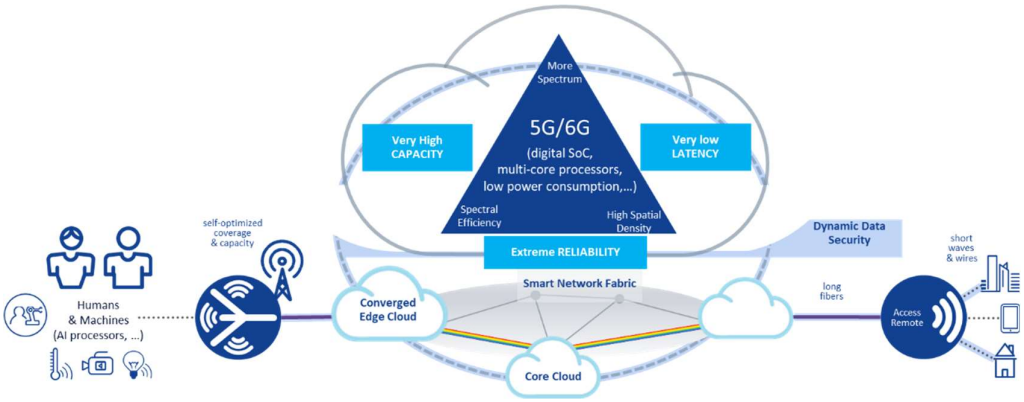

Figure 1: COREnect End-to-end System View.

The envisioned roadmap is created over three phases, as illustrated in Figure 2. During the first phase, the roadmap directions have been defined and roadmap input ("raw data") has been captured. During the second phase, the roadmap data is further processed, refined, and complemented, and also a common approach and structure are introduced across the different expert group descriptions. This uniform representation results in a clear representation of the key result/conclusions per expert group topic which enables to compare these findings across different expert group topics and market segments. During the third phase, we will define a common and consolidated roadmap proposition based on the material gathered during the proceeding phases. The current deliverable (D3.4) reports the outcome of the second phase and describes the **intermediate** COREnect roadmap proposition. The **final** roadmap proposition will be described in D3.6.

Figure 2: COREnect roadmap building timeline.

During the third phase of the roadmap definition sequence, the available roadmap material will be translated into actionable recommendations and guidelines for relevant private & public stakeholders and raise their awareness of the required investments. This activity will take place

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in T3.2 and WP4. Throughout the entire process, the proposed roadmap is defined in close interaction with internal and external experts. The expertise domains and the topic-clustering of the experts is described later in this document. The interactions with the experts are reported in D3.1, D3.2 and D3.5.

The current report introduces a uniform approach over the diverse topics covered by the experts. To maximize the potential social and business impact, we address four well-defined market segments, and we consider different impact timelines: in short term (<2026), medium term (2026-2030) and long term (>2030).

The outline of this document is as follows. Section 2 gives an overview of the strategic trends and potential business opportunities in the scope of COREnect. This section also indicates some of the key publications which act as a reference and baseline for our roadmap activities within COREnect. Section 3 introduces the implemented structure of expert groups, explains the uniform approach across all topics and introduces the applied market segmentation. This section also covers the roadmap data and identified strategic actions which have been drafted together with the experts. Section 4 draws the main conclusions.

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2. Strategic trends and opportunities

2.1. Context and objectives

Considering the full value chain, COREnect's main objective is to:

Develop a high-level strategic roadmap of core technologies for future connectivity systems and components, targeting next-generation European telecommunications networks and services (5G and beyond).

This roadmap proposal is being developed while considering the following factors:

- **The end goal of this industrial strategy is to support Europe's twin transition towards a green and digital future:** enabling our society to embrace digitalization in a sustainable way (from cost and power efficiency point of view) is a key societal challenge.
- **The necessity to strengthen Europe's strategy to differentiate and lead in its most important value chains while enabling the European ecosystem to adapt to a profound on-going value chain transformation:** it is mandatory to continue to innovate on "more than Moore" technologies to maintain Europe's leading role on key verticals. Today, advanced connectivity solution does not necessarily need chips processed in ≤ 5 nm node, but they will do so in the future. Moreover, the European ecosystem must also adapt to the value chain transformation induced by digitalization which requires to develop the relevant skills and technologies.
- **Aim for a realistic strategy keeping in mind that available economical resources are limited**: connectivity systems require a broad range of technologies which cannot be completely mastered by a single geographic area. This implies to clearly define key priorities in agreement with existing strengths.
- **The societal impact of the COVID pandemic:** the current pandemic has underlined the importance of connectivity infrastructure in the resilience of our society.
- **The COVID pandemic impact on key technologies supply chain and importance to secure Europe's sovereignty** (which does not mean autarky but allows for own decisions in Europe): the current supply chain issues underline the importance of cooperation with like-minded partners to support open, fair, and rules-based trade to reduce strategic dependencies.
- **The geopolitical trade tensions between the USA and China:** the export regulations on USA technologies have contributed to disruptions in the current supply chains. Moreover, Europe's current dependency on USA technologies hampers Europe to act independently and to take strong standpoints on business-related sovereignty topics.
- **The objective of the European Commission to enable Europe to produce 20% of the world's semiconductors by 2030 to meet future industry demand:** to secure European sovereignty, manufacturing of semiconductors in Europe should reflect the relative size of its domestic market and the strength of its industrial players on key verticals.
- **The necessity to reduce Europe's dependence on USA for EDA solutions, software and IP required to develop future connectivity systems:** the increased trade tensions between the USA and China highlighted Europe's vulnerability to USA technology; it indicated alarming sovereignty issues on connectivity technologies if extraterritorial rules are applied to European semiconductor players.
- **The necessity to bridge the current gap on advanced processor design to secure Europe's industrial strategy and digital sovereignty:** advanced computing is key to support the digitalization of our society. Today, Europe heavily relies on USA advanced computing technologies. This causes a critical dependency and might impact Europe's key ambition for open, ethical, trustworthy, and explainable AI and computing.

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The European Commission's objective to enable a fabrication plant to produce leading-edge technology (2 nm or even beyond) through selected partnerships to ensure security of supply, in the next 10 to 15 years: due to the importance of leading-edge semiconductor technologies to manufacture advanced computing chips, Europe has a role to play to enable a more diverse and consequently resilient supply chain to reduce its critical dependencies, while remaining open. It is quite likely that the advent of 6G will fire up the semiconductor market and its entire ecosystem. This is a strategic consideration but any decision on installing advanced CMOS manufacturing in Europe will need a detailed predictive market study.

Keeping in mind the previous context and objectives, we first propose a synthesis of the current position of Europe on the connectivity market to identify opportunities and gaps. We will then propose a global industry roadmap strategy which will be finally derived in concrete actions proposed by COREnect's expert groups.

2.2. Major challenges and opportunities related to future European connectivity systems and components

To identify Europe's major challenges or opportunities concerning connectivity technology, we start the discussion by a review of Europe's position in the overall value chain. As illustrated in Figure 3, Europe still holds a good share in materials and tools to produce electronic components. Europe's production share is, however, lower at levels such as electronic equipment, electronic boards, and electronic components.

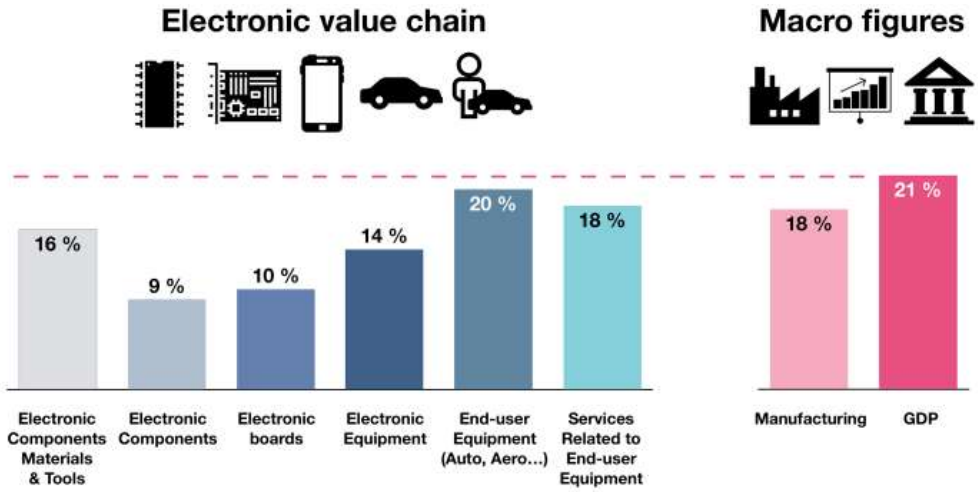

Figure 3: European share of the world production of the global electronic value chain [Dec20].

In Europe, the leading end-user segments are industrial electronics, aerospace defense and security, and automotive electronics. In the global electronics ecosystem, the leading segments are still the consumer mass markets (mobile phones, PCs). Consequently, Europe's share in the world production is also highest in those segments where Europe is strongest, as illustrated in Figure 4.

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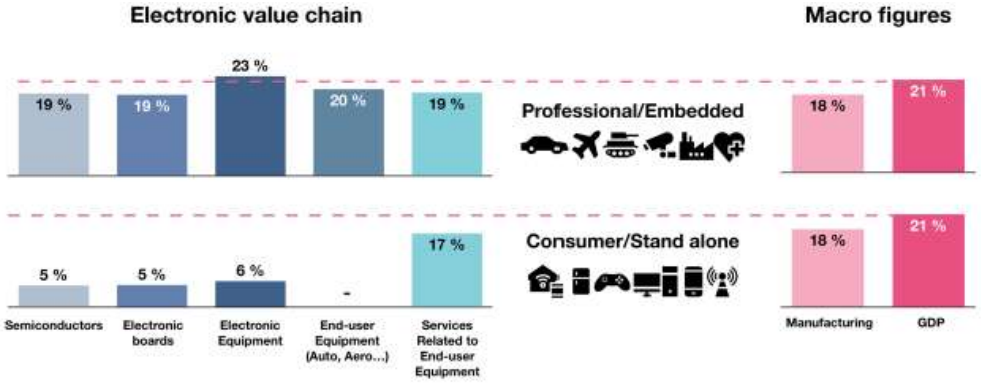

Figure 4: European share of the world production of the global electronic market focusing on professional/embedded and consumer electronic value chains [Dec20].

While Europe is just producing 9% of the overall electronic components (see Figure 3), its market share is 19% on the market it serves today as shown in Figure 4 (professional and embedded segments, the wireless infrastructure market being a good example with Ericsson and Nokia). This figure is in line with Europe's GDP. Since Europe hardly addresses the consumer market, the European ecosystem requires a moderated manufacturing capacity mainly focused on mature or derivate technology. For example: automotive represents today only about 10% [Gui21], but this is expected to increase in the coming years. The installed European semiconductor manufacturing capability to address Europe's key verticals is sized accordingly. As illustrated in Figure 5, Europe has a strong presence on 200 mm facilities (with STMicroelectronics and Infineon among the top 5 leaders) which is in line with the technologies required by the European ecosystem and value chain.

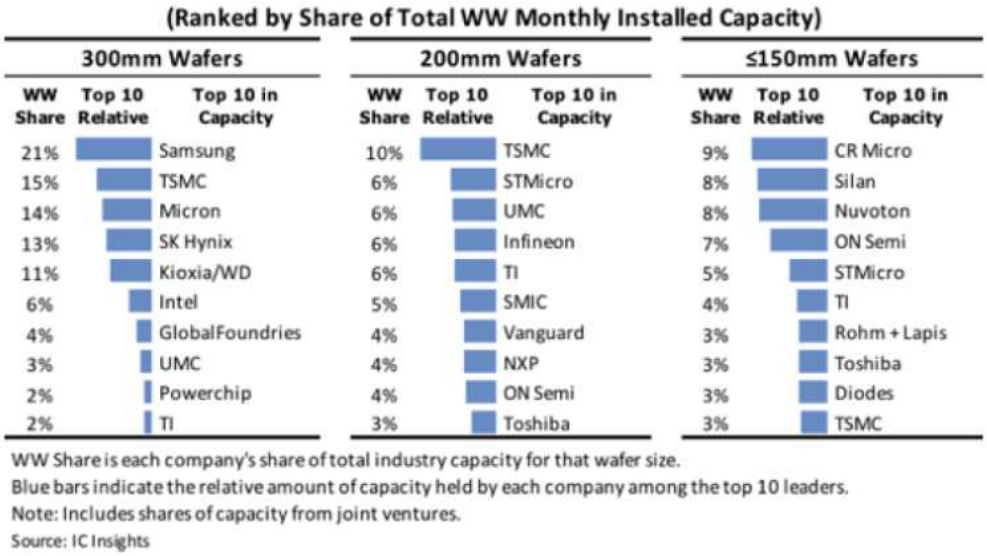

Figure 5: Installed capacity leaders in December 2020 by wafer size [EMS21].

The situation on 300 mm wafers manufacturing is completely different. On 300 mm, there is no European actor among the top 10 players. This is directly correlated with the European position on the market since the top 300 mm manufacturing players are addressing either memory (Samsung, Micron, SK Hynix, Kioxia) or advanced logic (Samsung, TSMC, Intel). These are two areas where Europe is hardly represented. As illustrated in Figure 6, the installed manufacturing

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capability of a given region directly correlates with the technology nodes required by the targeted markets of the associated value chain and ecosystem.

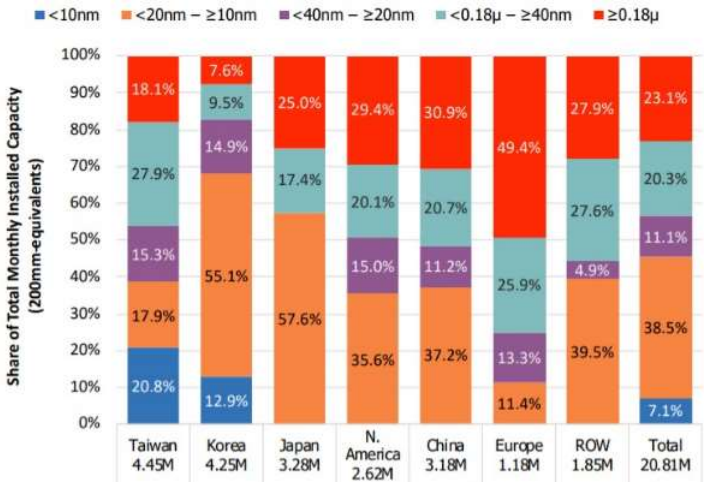

Figure 6: Monthly installed capacity for each geographic region in December 2020 [Nen21]. "ROW" means "rest of the world".

China, Japan, USA, and Korea have most of their installed capacity for technology ranging from > 10 nm to < 20 nm, which serves their memory production. On the other hand, 75% of Europe's installed capacity supports > 40 nm (50% for technologies > 180 nm) which serves its key verticals (automotive, industrial, health, …). Taiwan has a more balanced situation because TSMC's foundry business model clearly focusses on the most advanced nodes. TSMC's 1Q21 revenue, depicted in Figure 7, shows that the smaller nodes are driven by the smartphone and HPC business.

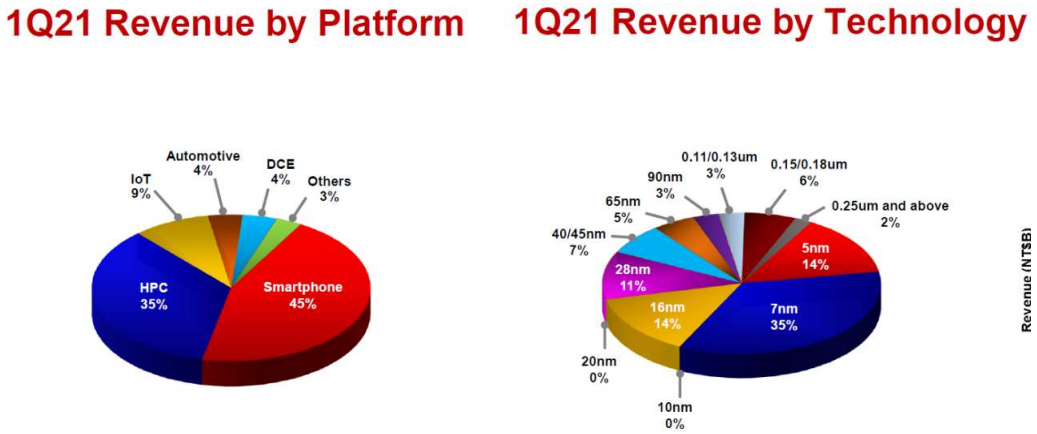

Figure 7: TSMC's 1Q21 revenue split per application and technology [TSM21].

We can also note that, while 7 nm and 5 nm represent 20% of TSMC's capacity, they generate ~50% of the revenue. This point is the foundation of TSMC's high-end foundry business positioning: by maintaining its leadership on advanced nodes and being the first to deliver volume manufacturing, it captures most part of the market value. This enables them to support the high CAPEX required to develop the next nodes and install the necessary capacity (TSMC's CAPEX in 2021 is set to 30 B$). Consequently, even a company able to offer equivalent

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technology and spending a large CAPEX such as SAMSUNG is today having a hard time to keep up with TSMC. From pure manufacturing side, the entry barrier is high and at short term, it may prove difficult for anyone to dispute the leadership of TSMC. Moreover, advanced manufacturing capability of 7 nm or beyond needs to come with a complex ecosystem that cannot be deployed on a very short term. Indeed, new fab players will have to build first the design enablement ecosystem (IPs, CAD flow, …) and prove to be a reliable partner able to deliver targeted performances in large volumes and in time.

While Huawei used to be TSMC's second largest customer just after Apple, the USA export restrictions have reshaped the landscape. Today, most TSMC key customers for 7 nm and 5 nm technologies are USA fabless companies. The only exceptions are Samsung and MediaTek. It illustrates a key weakness of the European fabless ecosystem. Since there are currently no large European fabless or system companies requiring high volumes in extremely scaled semiconductor technologies (< 7 nm node), the current industrial drive to develop such manufacturing capabilities shows to be rather limited. Moreover, given that China and USA are today leading in strategic topics such as AI, they are not expected to own the required manufacturing capability. As such, they are as dependent on the Taiwanese semiconductor technology.

However, the lack of < 20 nm node manufacturing capability in Europe does not mean that Europe refrains from this topic. Europe's strong position on semiconductor manufacturing equipment enables Europe to play a strategic role on the value chain. ASML is a good example since it is today the sole source of EUV lithographic scanner on the market. Figure 8 shows the EUV shipment forecast by customer and learns how leading foundries such as TSMC, Samsung and Intel are relying today on ASML (and consequently on European technology). This is a strong pledge for Europe.

Company	EUV shipments (unit)					
	2018	2019	2020	2021E	2022E	2023E
TSMC	**7**	**16**	**18**	**28**	**31**	**33**
Samsung	**3**	**5**	**8**	**9**	**14**	**15**
Intel	**4**	**3**	**3**	**2**	**3**	**5**
GlobalFoundries	1	0	0	0	0	0
Hynix	1	1	1	1	1	1
Micron	0	0	0	1	1	1
SMIC	0	0	0	0	0	0
Others	2	1	1	0	0	0
Total EUV shipments	**18**	**26**	**31**	**41**	**50**	**55**
EUV ASP (EUR mn)	**105**	**109**	**145**	**145**	**153**	**163**

Source: Mizuho Securities Equity Research Estimates

Figure 8: ASML EUV shipment forecast by customer.

The recent USA export restriction prevented Chinese companies to access to < 14 nm nodes by preventing USA vendors (such Applied Material, KLA, ...) and foundries to sell their USA-technology based products. This provides interesting perspectives concerning the position that Europe can adopt to safeguard its sovereignty and access to key technologies related to connectivity. Note, however, that so far, the US managed to pressure the Netherlands into barring China to acquire EUV equipment from ASML [woo21], so the degree of sovereignty that Europe could gain from its technology leadership in selected parts of the value chain is limited.

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Consequently, even if Europe does not own today the complete connectivity value chain, it still has a leading position on key topics. These topics include semiconductor manufacturing equipment, manufacturing of differentiated technologies, leading position on the wireless infrastructure market, etc.. This enables Europe to play a leading role in future connectivity technology development and ensure strategic maneuvering room by strengthening its partnership with other countries.

Worth mentioning is the leadership gained by the European RTOs in semiconductor science and engineering to seed the innovations in design architectures and manufacturing technologies. With the support of European funds incentives, basic research is stimulating and attracting industry R&D since their respective contributions are complementary and not redundant. For example, the FinFET transistor architecture, which has replaced the classical planar architecture in the recent CMOS generations, is the result of several decades of R&D collaborations. Similarly, the technology used by ASML for its flagship EUV lithography started in the 1980s on the use of soft x-rays.

Moreover, from pure manufacturing point of view, the importance of leading-edge technology nodes versus legacy ones must be put into perspective. Figure 9 shows that the capacity in leading-edge technology nodes will grow strongly in the coming 3 years while the legacy nodes will still represent a significant portion of the overall capacity (but also growing in absolute numbers).

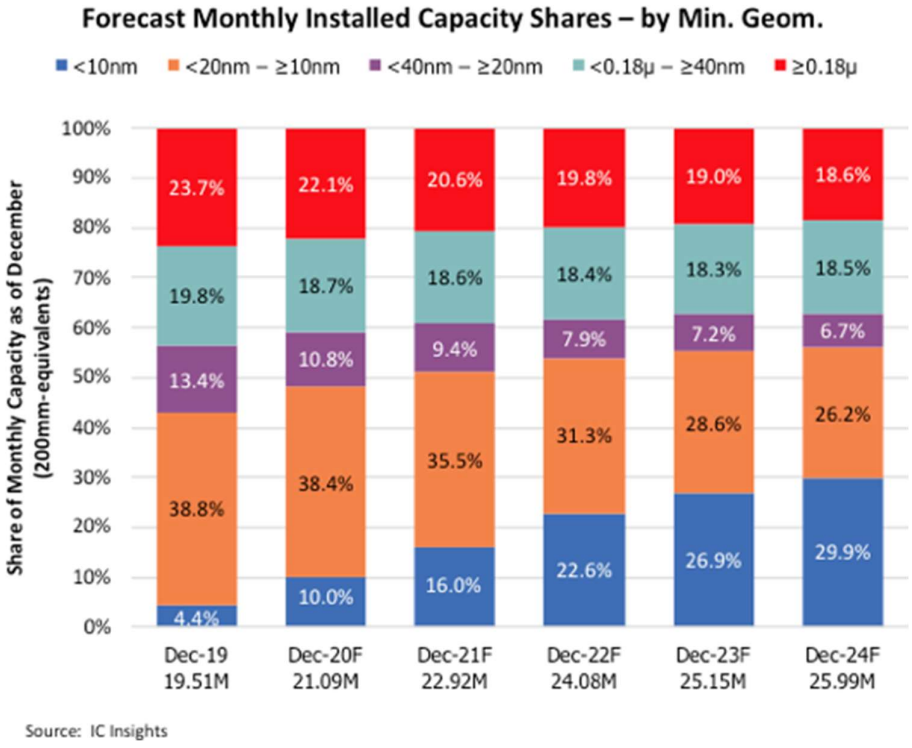

Figure 9: Wafer Capacity by Feature Size Shows [ICi20].

The growing trend of leading-edge technology capacity is mainly driven by consumer products such as smartphones. As illustrated in Figure 10, leading-edge technologies are used in 89 % of the smartphone's application processor and modem, whereas only 5% of the RF and connectivity chips use such technologies. Consequently, in the smartphone market, leading-

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edge nodes represent 27% of the overall chip area (~7.5M 12" wafer count/year) while legacy nodes are addressing the remaining 73% (~47M 8" wafer count/year).

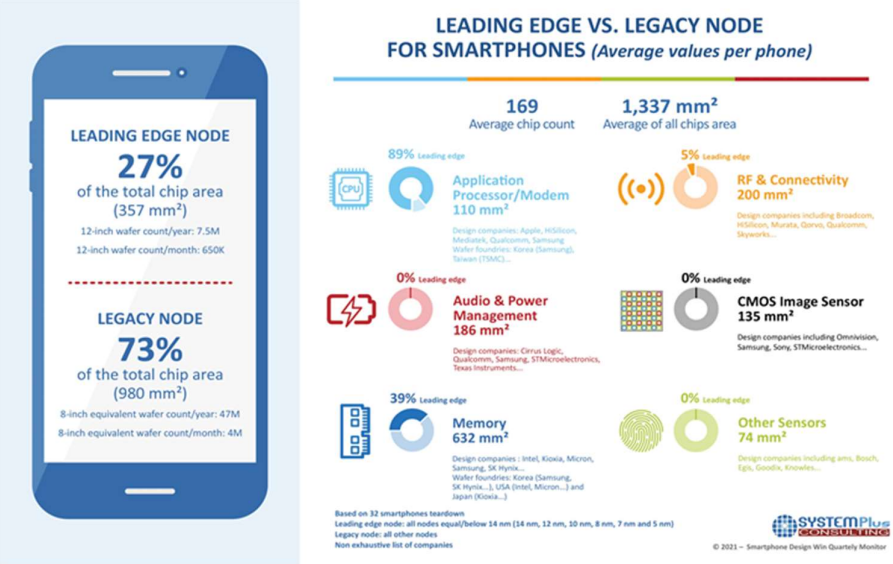

Figure 10: Leading edge versus legacy technology nodes used in smartphones [Sys21].

Given this persisting strong demand, the legacy technology node market will remain very active in the foreseeable future. The associated 200 mm installed capacity is expected to increase to record levels from 2020 to 2024, beating the last records seen in 2006 and 2007 (as illustrated in Figure 11). Moreover, one should also remember that European legacy technology node players are also transitioning to 300 mm fabs to increase even further installed capacity. Infineon's new 300 mm fab in Villach in Austria, STMicroelectronics' new 300 mm fabs in Agrate in Italy, Bosch's new 300 mm facility in Dresden in Germany and STMicroelectronics' 300 mm fab extension in Crolles in France are good examples of such actions.

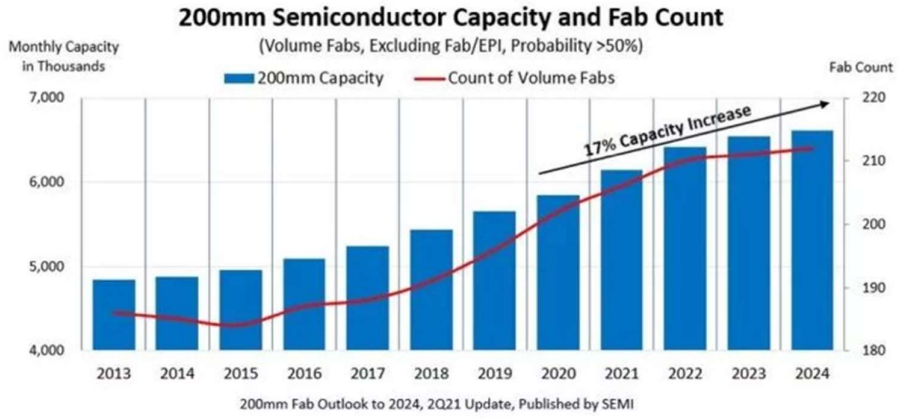

Figure 11: 200 mm semiconductor capacity and count of fabs [Fas21].

Put more simply, there is no opposition to be made between leading-edge and legacy technology nodes. Strengthening key partnerships within Europe may secure the technology access and the European sovereignty. Still, not owning the complete technology portfolio does not prevent Europe to capture a significant part of the semiconductor manufacturing chain. Europe's developed technologies and associated installed might, however, remain closely linked to needs

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of Europe's key verticals and the European overall position in the value chain (this comment also applies to other countries since for example TSMC is building a fab in the US targeting advanced 5 nm node to serve US fabless ecosystem while another one is being built in Japan targeting 28 nm node to serve the Japanese image sensor ecosystem). Having such technology and processing capacity, however, is likely to stimulate existing and to initiate new ecosystems in Europe.

2.3. Proposed Industry Roadmap Strategy: How should Europe address future connectivity technologies with a value-chain approach?

Based on the previous section, we can summarize European challenges and opportunities on connectivity technology to support its strategic agenda as follows:

Opportunities:

- Strong global position on wireless and wireline infrastructure markets and R&D
- Strategic link between core semiconductor technology capability and key verticals (automotive, industrial, space and defense, …)
- Combining those two assets makes Europe a strong contender to take a leading role towards 6G and beyond, while covering the entire value chain
- Europe has strong research in heterogeneous integration for many applications (high-performance computing, photonics, RF)
- In the industrial data market, that is several orders of magnitude bigger than the personal data market, Europe should not leave the storage and handling of these data (both 'central' and 'edge') to non-European companies.

Challenges:

- Digitalization modifies the European value chain, in which Europe risks to reduce its technological sovereignty. The rise of AI, for example, is likely to increase our dependency on USA technologies.
- Geopolitical tensions and trade restrictions impose an increased risk of disruption of the European supply chain. It is key for Europe to mitigate this risk through a more diverse and resilient supply chain.

With financial resources being limited, COREnect is proposing an industry roadmap with a 10- to 15-year timeline. This roadmap addresses different timeframes with a changing focus in terms of strategic investments, markets, and technological development.

Short term (2 years from now):

- **Strengthen areas where Europe is leading (BiCMOS, III-V, RF, analog, mixed signal, photonics ...) to secure its position and gain market share to ensure Europe to play a leading role for 6G:** Europe needs to continue to innovate on differentiated technologies where it leads today to secure its leadership. Transitioning from 200 mm to 300 mm fab manufacturing differentiated technologies is a key industrial challenge.
- **Secure access to < 7 nm CMOS technology:** Digitalization requires the know-how to design dedicated advanced computing chips. Europe needs to secure both the design capability as well as the access to a diverse and trustworthy supply chain.
- **Strengthen the education on IC design (both in analog/RF and digital):** To enable an appropriate pool of experts able to address European industrial players' needs but also make Europe an appealing place to invest. Contribute on open-source initiatives in processor core design IP (RISC-V) to differentiate on what today is openly available.

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- **Enable Europe to lead on future connectivity IPR generation, standardization actions while moving higher in the value chain:** Leveraging its current strength, Europe can play a leading role in the definition of 6G. Core technologies developed in Europe should also enable to develop more complex connectivity solutions (smart sensors enriched by AI features, more integrated 6G RF solutions, combination of radar and communication, …) and then capture more value.

Mid-term (5 years from now):

- **Define an aggressive timeline for the deployment of 6G at the scale of all EU state members:** while EU is today playing catch up on 5G deployment, it would be necessary to well anticipate this topic for 6G. Learning from what China did through MIIT's deployment policy, an aggressive agenda for 6G deployment at the scale of all EU member states will greatly boost EU initiatives and secure EU's capability to leverage connectivity infrastructure assets to serve its key verticals.
- **Strongly support module integration technologies (both design and fabrication) to combine components from a wide range of technologies (advanced digital and memory chips, but also legacy CMOS, FD-SOI, SOI, BiCMOS, III-V, photonics, sensors):** such approach will enable Europe to capture a higher portion of the value chain by delivering systems instead of components. Moreover, it may also allow viable solutions in markets that are not big enough to support the high development cost required by the smallest CMOS nodes. Instead, functionality could be implemented with multiple modularly designed chips in legacy technologies. This can enable defense industry to produce entirely in Europe exploring available production technologies even leading-edge nodes are not available.
- **Strengthen the European position on EDA, IP & software:** Creating an open and more diverse ecosystem is key to ensure a resilient supply chain and enable Europe to mitigate sovereignty risks. Chip design and EDA development, fields where USA leads, are expected to play a progressively larger role in driving performance improvements as transistor shrinkage slows.
- **Enable smartly positioned European fabless ecosystem:** To play a role in advanced computing chips (or modules) and to mitigate Europe's current dependency, a strong European fabless ecosystem is a mandatory starting point.

Long term (10 to 15 years from now):

- **Make Europe the IC design champion:** Europe must become the global IC design champion to ensure its position in connectivity system manufacturing and strong vertical sectors (application industry and domain knowledge as input for chip design) and to preserve their claimed value chain share.
- **Enable the establishment of < 2 nm CMOS manufacturing in Europe to support the created domestic market.** This can be implemented much sooner through partnerships with strong non-European players**.**

2.4. Reference material

Europe is not the only region of the world where roadmaps for electronics components and systems for future networks are derived. Even in Europe, while COREnect is specifically focusing on developing a roadmap of core technologies for future connectivity, relevant roadmapping information can be found in documents issued by other groups, addressing a wider or different but related application scope. Table 1 gives a selected list of those documents.

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Table 1: Other relevant roadmapping initiatives.

Document name	Related section	Date
ECS Strategic Research and Innovation Agenda[1]	Section 2.2 connectivity	01/2021
International Roadmap for Devices and Systems[2]	Focus team "Outside System Connectivity"	2020
5G ACIA white paper[3]		02/2019
Decadal Plan for Semiconductors - SRC[4]	Chapter 3: New Trajectories for Communication	01/2021
Webinar "New Apps and New Possibilities: How 5G Will Dramatically Change the Semiconductor Industry"[5]		07/2020
"Smart networks in the context of NGI" from NetworldEurope ETP[6]		01/2021
NTT DOCOMO White Paper: "5G Evolution and 6G"[7]		02/2021

In addition to these roadmapping activities, the COREnect consortium could evidence the intensity of the current debate regarding strategic digital autonomy in various regions of the world, translating into legislative actions and/or investment decisions. Below is a brief overview across several countries.

Legislative activities in the USA

Responding to concerns, the USA is increasingly reliant on imported microelectronics, Congress enacted the bipartisan *Creating Helpful Incentives for Producing Semiconductors (CHIPS) for America Act*[8] in December 2021 as part of the National Defence Authorization Act, its annual defence policy update. The legislation authorizes an array of R&D initiatives as well as a subsidy program for domestic semiconductor manufacturers. However, while early versions of the CHIPS for America Act envisioned spending more than ten billion dollars over five years, the enacted version makes no specific funding recommendations for either the overall initiative or its component elements. In any case, actual funding for them will have to be provided through separate spending legislation.

On February 24, 2021, the President signed E.O. 14017, directing a whole-of-government approach to assessing vulnerabilities in, and strengthening the resilience of, critical supply chains. This resulted in the release, on June 8, 2021, of findings from this comprehensive 100-day supply chain assessments for four critical products: semiconductor manufacturing and advanced packaging; large capacity batteries; critical minerals and materials; and pharmaceuticals and active pharmaceutical ingredients. Of specific interest for the COREnect project are the key findings regarding semiconductor manufacturing and advanced packaging, namely:

- Promote investment, transparency, and collaboration in partnership with industry, to address the current shortage,

[1] https://aeneas-office.org/pdf/sria-2021/

[2] https://irds.ieee.org/editions/2020

[3] https://5g-acia.org/wp-content/uploads/2021/04/WP_5G_for_Connected_Industries_and_Automation_Download_19.03.19.pdf

[4] www.src.org/about/decadal-plan/

[5] https://bit.ly/3iXZSyP

[6] https://bscw.5g-ppp.eu/pub/bscw.cgi/d392313/Annex%20v2.3%20-%20Public.pdf

[7] www.nttdocomo.co.jp/english/binary/pdf/corporate/technology/whitepaper_6g/DOCOMO_6G_White_PaperEN_v3.0.pdf

[8] www.aip.org/sites/default/files/aipcorp/images/fyi/pdf/chips-for-america-act-final.pdf

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- Fully fund the chips for America provisions to promote long-term US leadership,
- Strengthen the domestic semiconductor manufacturing ecosystem,
- Support SMEs and disadvantaged firms along the supply chain to enhance innovation,
- Build a talent pipeline,
- Work with allies and partners to build resilience,
- Protect the US technological advantage.

In particular, the report states that "*as an initial step, Congress should fund the chips provisions with at least $50 billion in funding*". Details can be found in the document entitled *100-day supply-chain review report*[9].

To decrease their dependency on foreign-based semiconductor production, the USA is also attracting foreign investment. A case in point is the Taiwanese company TSMC which broke ground in June 2021 on its $12 billion semiconductor fab in Arizona[10]. Likewise, Samsung Foundry has filed documents with authorities in Arizona, New York, and Texas seeking to build a leading-edge semiconductor manufacturing facility in the USA. The potential fab near Austin, Texas, is expected to cost over $17 billion and to create 1,800 jobs[11].

Finally, the USA is actively using export control laws to prevent mainland China from developing sub-10 nm node technology, for example by barring ASML to sell Extreme UV equipment to Chinese semiconductor manufacturers, and even trying to extend that ban to older, Deep UV equipment[12].

Mainland China

In 2015, mainland China released its "Made in China 2025" initiative, which included the ambitious goal of reaching 70 per cent self-sufficiency goal for semiconductor production. However, they are so far falling very short of being on a trajectory meeting that target: IC production in China, including output by both foreign and domestic players, only accounted for 15.7% of its $125 billion chip market in 2019. If only companies with headquarters in China are considered, their production accounted for just 6.1% of China's total IC market that year. At its current pace China will only achieve one third of its goal.

Nevertheless, mainland China main semiconductor manufacturer, SMIC, has been increasing its R&D expenditures rather rapidly in recent years. In 2014, the company spent $189.7 million, or 9.5% of revenue, on research and development. Five years later, in 2019, the company spent $629 million, or 20.7% of revenue on R&D. In parallel, its CAPEX was expected to reach $4.3 billion in 2020[13]. On March 31st, 2021, SMIC announced 2020 sales of $3.9 billion and gross profit of $0.9 billion, while the debt-to-equity ratio "remained low"[14]. A large CAPEX can only be achieved via capital injection from the shareholders. Since by late 2018 the Chinese government controlled at least 46.36% of the company, this corresponds to a significant amount of public support.

[9] https://www.whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf

[10] https://www.datacenterdynamics.com/en/news/tsmc-starts-work-on-12bn-arizona-semiconductor-fab-gets-funding-for-japanese-chip-rd/

[11] https://www.anandtech.com/show/16483/samsung-in-the-usa-a-17-billion-usd-fab-by-late-2023

[12] https://www.techzine.eu/news/infrastructure/56766/usa-tries-to-prevent-all-export-of-asml-machines-to-china/

[13] https://www.eetimes.com/smic-advanced-process-technologies-and-govt-funding-part-2

[14] https://www.smics.com/en/site/news_read/7809

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Japan

Similar to the USA, Japan is also discussing with TSMC's towards the building of a chip fab in Kumamoto, which would be TSMC first Japanese semiconductor factory[15].

South Korea

Finally, the South Korean government announced on May 13th, 2021, a plan by companies to invest 510 trillion won ($451 billion) throughout 2030 and beefed-up tax benefits to boost chipmakers' competitiveness amid a critical global shortage of the key components. "*Our government will unite with companies to form a semiconductor powerhouse. We will support companies concretely.*" said President Moon Jae-in[16].

As part of the effort, the Finance Ministry said it will raise the tax deduction ratio for semiconductor research and development investments by big companies to 40% from the current 30%, paving the way for Samsung and SK Hynix to benefit from the eased financial burden. The chipmakers also will enjoy higher deductions for investments in facilities, as the government is doubling that ratio to 6%, the ministry said.

[15] https://www.datacenterdynamics.com/en/news/tsmc-considers-chip-fab-in-kumamoto-its-first-japanese-semiconductor-factory/

[16] https://asia.nikkei.com/Business/Tech/Semiconductors/South-Korea-plans-to-invest-450bn-to-become-chip-powerhouse

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3. Strategic roadmap foundation

Based on initially identified COREnect end-to-end system view together with value chain consideration, COREnect organizes three COREnect Expert Groups to address the industry roadmaps in three strategic focus areas:

- Expert Group #1 Compute and Store
- Expert Group #2 Connect and Communicate
- Expert Group #3 Sense and Power

Today, the expert groups consist of 104 experts from industry, SME's, research institutes, universities, and associations. 61 experts are consortium members, and 44 experts are from outside the consortium. Expert Group #1 and Expert Group # 3 each consists of 20 members and Expert Group #2 contains 65 members and Expert Group # 3 consists of 20 members. COREnect remains open for new experts via published calls (https://www.corenect.eu/news/call-for-experts). In this way, we keep on maintaining an optimal scientific, organizational, and societal balance. For each expert group, a Chair and Vice-Chair have been selected by the COREnect consortium with the responsibility to coordinate these groups. As a result of several public workshops and focused meetings and brainstorm discussions, the experts aligned their views on Europe's major challenges and opportunities. Combining their specialist knowledge, COREnect benefits from broad insights and vision into crucial fields that require our attention and, thus, address the upcoming challenges in Europe regarding 5G and beyond. Altogether, capturing and crystallizing the discussions, the three expert groups are cooperatively developing the COREnect industry roadmap.

Although each Expert Group is focusing on a defined strategic area, one can find many overlapping topics within this holistic approach.

Security and energy efficiency are cross-cutting design considerations in the COREnect technical vision and inherently the common work of Expert Groups. Therefore, the sphere of ***Energy Efficient, Green Communication Electronics*** will be equally covered in the chapters dedicated to the expert groups. Therein, advanced computation and sustainable fabrication are going to be examined from the perspective of the device itself (EG1), the transceivers (EG2), as well as from the sensors and power management (EG3) point of view.

Regarding 5G/6G application areas, security and trustworthiness are both a focus for several stakeholders. Therefore, technologies to cope with untrusted third-party IP (EG1), telecommunication hardware and software (EG2) and failure detection and security technologies (EG3) are contributing to the question of how to derive ***Electronics for Trustworthy Communication*** in 6G and beyond. Regarding the technical aspects of the European sovereignty and its ecosystem, the key question is whether a whole European value chain including the tools and knowledge is feasible, required, and how it can be realized.

An integrated approach of ***Future Core-Technologies and Integration*** throughout all three expert group chapters is going to highlight the areas in packaging, materials, semiconductors, production, and assembly that can bring Europe forward towards a more inclusive and carbon-neutral society. For instance, multi-chip modules (MCM) and the integration of memory chiplets (EG1), semiconductor trade-offs for wireless and wireline transceivers (EG2), or heterogeneous integration and the semiconductor processing technology landscape (EG3) and its opportunities for Europe are being reflected on in each chapter. Social inclusion with new user interfaces,

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knowledge, education and job generation, and the general orientation towards megatrends (e.g., demographic change, global warming) will equally play a role, guiding the proposed strategies towards a common goal.

To **maximize the potential social and business impact**, we address four market segments across the three strategic focus areas. This approach forces to consider the composition, strength, and resilience of entire value chains, which is essential to guarantee a sustainable technological sovereignty. These four market segments described more in detail in Table 2.

Table 2: Overview of the market segments, used across the different strategic focus areas.

Connectivity infrastructure
Description: Electrical infrastructure that enables network connectivity, communication, operations, computing capabilities and network management. *Scope:* Wireless access, fronthaul and backhaul network infrastructure. Broadband base stations, radio units, access points and routers. Wired (optical, electrical, ...) access, fronthaul, backhaul, metro, core and datacenter network infrastructure. *Technical Requirements:* Mild constraint on cost, size and power consumption Trustworthy: secure, safe and privacy preserving *Targeted customer group(s):* Mobile, private, and virtual network operators. Data center owners. *Volume:* Tens of million, linear growth
Consumer grade connectivity
Description: Mobile devices that have sophisticated computing capability for everyday use. *Scope:* Mobile phones, smart watches, and other future portable devices. AR/XR devices. Connected domestic robotics. *Technical Requirements:* Constraints on cost, size and power consumption Trustworthy: secure, safe and privacy preserving *Targeted customer group(s):* Consumers, business uses, consumer healthcare *Volume:* Thousands, millions, billions (depending on application), exponential growth
Industry grade connectivity
Description: Low-cost and low power devices for vertical applications especially in industrial environments *Scope:* IIoT, sensors, private and deterministic networks, edge computing, intelligent devices *Technical Requirements:* Extremely low power, low cost Increased security of the data *Targeted customer group(s):* Industry 4.0, agriculture, digital healthcare, energy *Volume:* Millions, exponential growth
Automotive connectivity
Description: High-performance and low power devices for automotive applications operating in unconstrained mobility spaces and public environments *Scope:* V2X (WLAN, cellular), sensors, mobile/multi-access edge computing, intelligent devices *Technical Requirements:* Extremely low power, low cost

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High demand on security of the data and latency

Targeted customer group(s):

Connected and automated mobility (automotive, shipping, rail), parcel logistics and shipping

Volume:

Millions, exponential growth

These market segments are addressed by the experts of the three strategic focus areas, if relevant. Some expert groups will create sub-categories within a market segment for increased focus or to highlight some differentiation within a particular market segment. For each market segment or sub-category, a SWOT (strengths, weaknesses, opportunity, threats) analysis is performed, and the related strategic actions are identified. Having this information for each market segment within each key strategic focus area eases the aggregation and the definition of a global roadmap proposition as to be able to extract global recommendations.

The following sub-sections describe the experts' views of the three key strategic focus areas. Each expert group addresses the market segments described above, shows the related SWOT analysis result, and suggests the identified strategic actions across the impact timeline. The more technical justification is described in the research area subsections, which sources from D3.3.

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3.1. EG1: compute and store

3.1.1. Introduction

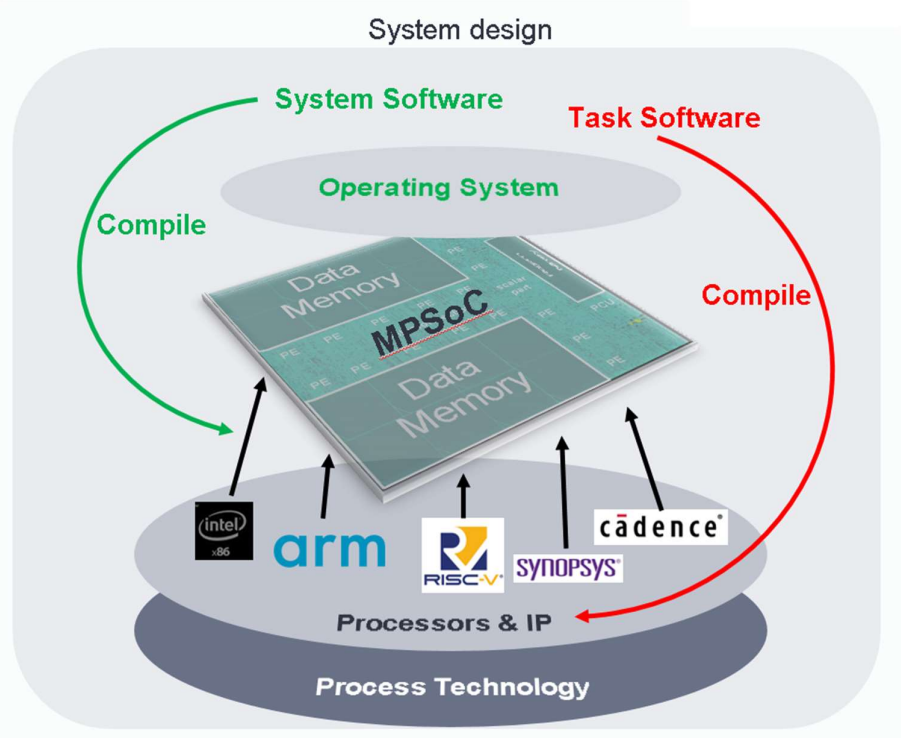

Figure 12: Common architecture of computing systems.

For 5G and beyond, ever more performant digital computing platforms and components will be required. However, Europe is becoming increasingly dependent on non-European supply for these components and systems. This makes the European supply chain highly susceptible to disruptions such as trade wars. Expert Group 1 (EG1) therefore investigates the role of computing and storage solutions for Europe's 5G and 6G sovereignty.

EG1 identifies key technologies and strategic actions that enable Europe to build trustworthy and competitive solutions in the four market segments addressed by COREnect:

1. Connectivity Infrastructure
2. Consumer Grade Connectivity
3. Industrial Grade Connectivity
4. Automotive Connectivity

While the architecture of programmable computing platforms, as depicted in Figure 12, is similar across the market segments, the market segments differ in the KPIs and the operating constraints they impose on the platform and each of its components. We analyze, in addition to these requirements, for each market segment prospective trends and Europe's strengths, weaknesses, opportunities, and threats (SWOT) and recommend key strategic actions in sections 3.1.2-3.1.5.

The market analysis is supported by a technology-oriented description of the main research areas in computing and storage in section 3.1.6. It encompasses the 5G/6G system architecture, process technologies, instruction set architectures (ISAs), memory and storage, multi-processor

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system on a chip (MPSoC) design, and a novel operating system (OS) framework. We conclude in section 3.1.7 with a summary of the key strategic actions relevant for all or most market segments and research areas.

3.1.2. Connectivity infrastructure

While RAN and routing equipment, packet-core servers, and datacenters are not necessarily mission critical, i.e. a failure is unlikely to have fatal consequences, they still require an extraordinary level of reliability and availability and a high QoS. To examine this, we will have a closer look at the RAN workload.

Figure 13 shows a logical architecture of the RAN. It is a refinement of Fig. 6.1-1 of 3GPP TS 38.401. The additional interfaces (in green) are specific to the O-RAN Alliance proposal but can also be proprietary.

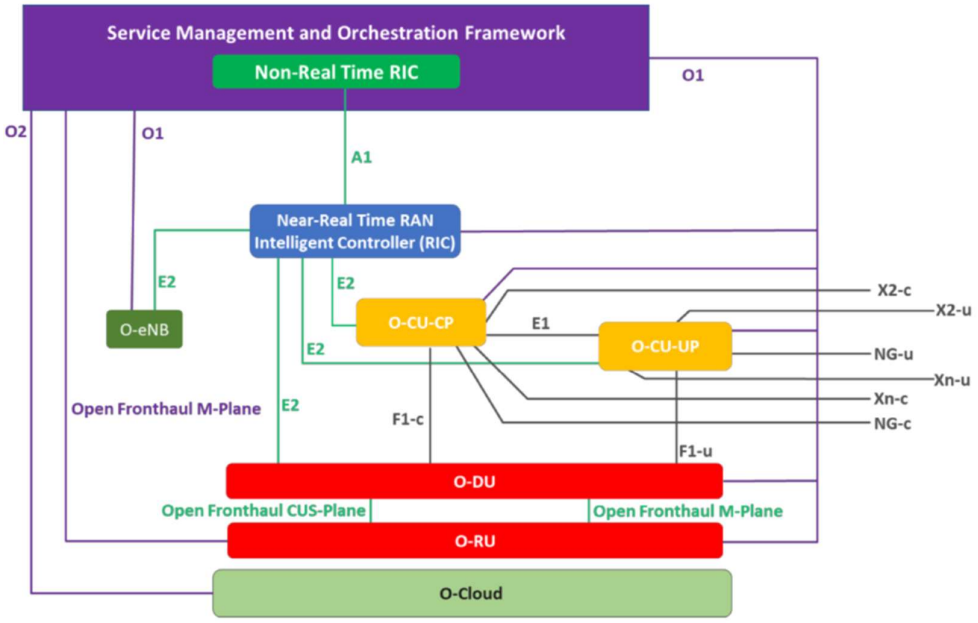

Figure 13: RAN overall logic architecture with O-RAN specific interfaces depicted in green [ORA19].

Most of the RAN compute load is in the radio (RU), central (CU) and distributed units (DU), where (most of) the L1-L3 signal processing occurs. This workload:

- addresses multiple standards, including (3G), 4G, and 5G
- is complex, highly dynamic, and involves a large number and large variety of different tasks
- is measured in Peta-ops/sec
- has to meet extreme latency constraints, measured in micro-seconds per task
- must support so-called macro network blocks, including their activation and termination

In addition, some application functions may migrate in part to the base stations (close to the O-CU and final IoT edge AI devices).

A result of these high-performance requirements is the use of discrete components. Memories, for example, are usually stand-alone components connected via DDR interface, because the data requirements for processing and storage in this market segment cannot be met by embedded

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memories. The RAN compute platform will also likely be made up of multiple system-on-chips (SoCs), as described in section 3.1.6.1.

3.1.2.1. Short term impact (<2026)

The interfaces and protocols to be used in infrastructure equipment in 5-10 years will be standardized in the next couple of years. Europe should continue to ensure activities in standardization groups such as JEDEC and PCI-SIG. Since Europe is a big market globally, it has good weight in standardization bodies. It can also steer future technology trends by defining and enforcing regulations which ensure security and privacy. ISAs (c.f. section 3.1.6.3), MPSoCs (c.f. section 3.1.6.5) and Operating Systems (c.f. section 3.1.6.6) that are developed in Europe right now and that consider these issues will otherwise not gain any traction. To protect ideas that might be used in future components and systems, it is also wise to protect European patents in the field of computing and storage.

3.1.2.2. Medium term impact (2026-2030)

Market adoption of products resulting from research needs to be supported. There is ongoing research on:

- Change/optimization of the memory hierarchy to replace DRAM with faster and more energy-efficient alternatives such embedded dynamic random-access memory (eDRAM) or embedded non-volatile memory (eNVM) (c.f. section 3.1.4.1 and section 3.1.6.4)
- Co-design of applications and the memory system to increase energy efficiency and identify opportunities for component-level innovation
- Definition of an interconnection of multiple MPSoCs for 5G/6G applications such as beamforming which require close and synchronous cooperation. These will likely go beyond near-memory standards or classical networking interfaces.
- Creation of new MPSoC codesign and optimization methodologies to enable trade-offs between security, power, performance, and time-predictability to avoid massive over-provisioning of computing capabilities and the memory hierarchy (c.f. section 3.1.6.4, 3.1.6.6)
- A new generation of dedicated AI chips and their integration in aforementioned MPSoC architectures
- Open European hypervisor solutions (c.f. section 3.1.6.6)
- Isolation mechanisms for sensitive pieces of data in the wireless network (e.g., blur a picture in HW close to the camera sensor before it is sent via the RAN)

Since the 6G standardization process is expected to take place in this time frame, Europe should use its weight to ensure that 6G is GDPR-compliant “by nature” by considering the results of these research efforts.

3.1.2.3. Long term impact (>2030)

With its strong position in the infrastructure market and research, its expertise in material science, and the existing fabrication capacity, Europe might become an IC design and fabrication powerhouse. If it is ensured that European companies have some advantage from buying chips in Europe, Europe can

- Develop new process technologies for memory and specific applications
- Fabricate solutions with heterogenous 3D integration (c.f. section 3.1.6.2)

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- Sell IP for memory and MPSoC inside and outside of Europe

Europe's strong secure OS and virtualization technology base, established by multiple existing SMEs, enables Europe to develop an open cloud infrastructure for a scalable edge-to-cloud compute continuum based on open interfaces, and a European cloud hypervisor (c.f. section 3.1.6.6).

3.1.2.4. European strategic position and potential - SWOT

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• 2 out of 3 of major telecommunication infrastructure vendors • Vertical industry ready for adoption • Strong OS, security know-how in SMEs and academia • Existing European hypervisor implementations, ready for adoption • Competence in research and patent portfolio in memory and storage (TRL<=5)	• Lack of strong Cloud providers in Europe • Later deployment of newest technology compared to other regions • Weak European industry presence and less skilled personnel in communications computing domain • Investment in base-level software infrastructure missing • Unaligned activities among European researchers in memory and storage • No European products in memory and storage (no TRL>5) • Little Influence on software landscape
Opportunities	*Threats*
• Digital infrastructure as foundation of society and economy • Europe is strong in secure operating systems and hypervisors; implementations exist • Collaboration with datacenter and other infrastructure equipment companies to design own use-case optimized memory solutions	• EU unable to keep pace with US and China on AI • EU overly dependent on supplier from other continents and vulnerable for any disruption and potential security breach • No capability on < 7 nm manufacturing which is critical for infrastructure products • O-RAN as an advantage for non-European silicon companies • When we use external fabs, we give away a lot of information, e.g., about our memory designs

3.1.2.5. Identified key strategic actions

Short term (<2026)
• Ensure activity in JEDEC and PCI-SIG • Implement local datacenter/cloud infrastructure in Europe • Develop ISA extensions to enable inclusion of programmable accelerators • Develop an MPSoC meta-level description standard for integration of third-party IPs • Protect European patents in computing and storage • Secure access to < 7 nm CMOS technology • Shift public funding from materials to circuits • Strengthen Europe's industry capability on AI
Medium term (2026-2030)
• Develop and deploy a modular secure OS framework, European cloud and hypervisor technology • Involve independent certification bodies to ensure evaluation of OS against European security and privacy standards • Build datacenters in Europe • Ensure secure and privacy-respecting local storage in Europe • Invest in education in relevant technologies (systems, security, AI)

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• Invest in 2.5D and 3D packaging • Support market adaption of existing open European hypervisor solutions • Push for isolation mechanisms for sensitive pieces of data in the 6G standard
Long term (>2030)
• Sell datacenter services (e.g., storage) outside Europe • Establish leadings edge technology source in Europe • 7G

3.1.3. Consumer grade connectivity

Arguably, consumer grade connectivity is the market segment where Europe is the furthest behind in computing and storage. Consumers usually expect their devices to be of low cost, the UI (User Interface) to be familiar and software to be backwards-compatible. The factors make it hard to establish new ecosystems. For example, even a technology giant like Microsoft failed to establish a third mobile OS ecosystem besides Android and iOS. On the other hand, European customers tend to value privacy and security. This presents an opportunity for a European isolation layer that ensures security and privacy while running established eco-systems. This is definitely possible for the Android ecosystem; however, iOS devices are a closed eco-system without the option to control the hardware. Prerequisite is definitely to trust/control the hardware (c.f. section 3.1.6.3, 3.1.6.5) such that the OS/base-level software (c.f. section 3.1.6.6) can rely on the hardware to provide isolation.

There is also the need of designing a scalable modem for UE (User Equipment) as described in section 3.1.6.1. Here, the main challenge is the wide range of requirements that need to be satisfied because of many standards and use cases.

3.1.3.1. Short term impact (<2026)

To foster the development of secure and private consumer devices, it is beneficial to put emphasis on the regulatory part. The EU should define and enforce regulations for consumer markets (e.g., safety related standards), set appropriate IPR targets, and invest into execution of these. These measures may create an appropriate level of interest among universities, institutions, and companies to focus on consumer-grade computation and storage R&I, at least on the architecture level. Possible technologies, where Europe can get an advantage are:

- Storage-over-radio network with Ericsson and Nokia as leads
- Development of competitive open-source hardware
- Hardware that enforces trust relations between MPSoC components. Trust is necessary to allow running multiple applications on the processors in a mobile device and the OS manages these trust relations. The EU is already very strong in security especially cryptography.
- Optimized MPSoC co-design to enable tradeoff between security, power, performance and time-predictability. Here, the EU can leverage its competence designing flexible interconnects for MPSoCs (e.g., STM) and can create the addition of new system components and IP cores that support the real-time capability requirements of 5G/6G.
- Recycling of memory components. As consumer-grade products have usually a short life cycle, memory components can be unsoldered, tested, and refurbished.
- Hybrid memories like eDRAM and eNVM
- (3D) integration of eNVM and coupling to SRAM

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3.1.3.2. Medium term impact (2026-2030)

In the medium-term, several European research efforts might begin to find their way into consumer grade devices if they are properly funded. These research efforts include:

- 3D integration
- Transition from the classic memory hierarchy to non-von-Neumann architecture (e.g., in-memory processing)
- ISA extensions and accelerators for compute intensive parts in the mobile device
- New hardware/software co-design methodologies of MPSoCs for the 5G/6G context through a higher-level software stack definition
- Low-level software layer for isolation and data protection that ensures that existing mobile eco-system run isolated.
- Accessible hardware platforms and low-level system stacks to enable replacing individual components with European-grown alternatives (the "IBM-PC" of mobile platforms)

3.1.3.3. Long term impact (>2030)

Europe has experience in application-level OS development for telecommunication systems. This experience should be used to go beyond classic coordination languages and system design methods based on execution models and dataflows. EG1 envisions a new OS-based software stack definition through higher-level abstraction methods for Hardware/Software co-design of MPSoCs for the 5G/6G context.

Europe can also gain independence by being able to R&I on embedded memory technology levels and productizing memory technology IP.

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3.1.3.4. European strategic position and potential - SWOT

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• Strong research ecosystem in R&D centers and universities • OS technology available for securing / virtualizing mobile devices (has been proven) • Europe is strong in memory (storage) innovation	• No strong European companies for consumer devices • Difficult access to venture capital • Europe is weak in selling its memory (storage) innovation • The CMOS race is already lost for Europe • Europe still cannot fabricate FinFET
• Base new systems on European values and ethical principles to improve security and user-controlled privacy, which is becoming attractive also for other regions • Europe is strong in secure operating systems, European tech can be used to secure devices • Master design of memory IP and MPSoCs • Accelerate innovation in 3D integration • Wireless storage becomes increasingly attractive • Master fabrication of advanced FinFET • Support Research on a new OS-based software stack with high level of abstraction	• Foreign companies (largely) controlling European data on mobile devices • Diminishing access to IP • Acquisition of innovative European SMEs by non-European technology giants • High entry barrier
Opportunities	*Threats*

3.1.3.5. Identified key strategic actions

Short term (<2026)
• Develop an MPSoC meta-level description standard for trustworthy integration of third-party IP • Support development of open and accessible hardware • Define and enforce regulations for consumer markets (e.g., safety related standards) • Plan access to design tools, license costs, IP costs • Set appropriate IPR targets • Reconsider the collaboration and patent strategies in European academia, research institutions, corporations • Investigate storage-over-radio network
Medium term (2026-2030)
• Push for accessible hardware platforms and low-level system stacks to enable replacing individual components with European-grown alternatives • Facilitate the transition from the classic memory hierarchy used in von Neumann computers to memory used in emerging non-von-Neumann computers • Invest in 2.5D and 3D packaging • Push for isolation mechanisms for sensitive pieces of data in the 6G standard
Long term (>2030)
• Design a new OS-based software stack definition through higher-level abstraction methods • Address research questions related to eNVM improvements (c.f. section 3.1.4) • Productize memory technology IP

3.1.4. Industrial grade connectivity

Modern industrial production processes (dubbed “industry 4.0”) make extensive use of connectivity for coordination and control. This involves embedded devices forming an “internet of things” (IoT) doing sensor data and communications signal processing. As failure or

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disruptions may lead to expensive production outages, the compute platform is mission critical. Its requirements are

- Safety against malicious and accidental attacks
- Low latency or even real-time capability
- Scalability
- Low energy consumption.

This market segments also includes non-industrial applications that share similar requirements like home automation ("smart home") or aerospace applications (e.g., radiation-hardened processors by Cobham Gaisler).

3.1.4.1. Short term impact (<2026)

For industrial grade microcontrollers (but also for consumer and automotive devices), eNVMs are of high interest because of their low energy consumption and high speed. For security, memory IP should be designed in Europe. Companies like GlobalFoundries and STMicroelectronics are already selling magnetoresistive random-access memory (MRAM) or phase-change memory (PCM), respectively. These existing eNVM technologies may be improved in terms of energy efficiency and endurance. Several European research and technology organizations (RTOs) like CEA and IMEC are present in eNVM research. An industrial transfer of new eNVM technologies such as ferroelectric random-access memory (FeRAM), metal oxide resistive random-access memory (OxRAM) and new MRAM needs to be started.

The wide range of use cases calls for methodologies to efficiently design optimized MPSoCs to enable tradeoffs between security, power and performance and to enable real-time capabilities. Start-ups and SMEs with this intent can be fostered by establishing "digital design kitchens": centers with offices for such companies where they can innovate the end-product and the chip platform in parallel.

Embedded devices seldom run heavy operating systems because of the high overhead. An open low-resource OS framework therefore needs to be developed and researched. This framework also needs a supporting organization that maintains it, especially with regards to security and safety.

3.1.4.2. Medium term impact (2026-2030)

In this time frame it is crucial to reinforce the link between research and production and confirm that the aforementioned new memory technologies (FeRAM, OxRAM, new MRAM) have been transferred to industry. Research opportunities for eNVM that are becoming relevant in the medium term are new crossbar architectures, new physical unclonable functions (PUFs) and random-telegraph-noise-based (RTN) fingerprinting, and secure memories.

If successful, the aforementioned research efforts in MPSoC design methodologies and a low-resource OS framework can be offered commercially as competitive options for designing constraint devices.

3.1.4.3. Long term impact (>2030)

Ultimately, Europe might gain a stronghold in memories, MPSoC, and OS and sell solutions with high energy efficiency for IoT, BT, industry 4.0, smart home, aerospace, etc. as it has relevant

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fabs and hardware and software companies, as well as the industries that need these solutions in security, home, IoT, etc.

3.1.4.4. European strategic position and potential - SWOT

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• Strong industry position on IoT, sensors and automotive electronics • Strong edge processor, OS, security know-how in SMEs and academia • Industry 4.0 • Existing industrial solutions in eNVM • Stronger position in eNVM with larger IP and patent portfolio	• AI edge processing • Reliance on consumer-area products • Reliance on outside leading-edge process technologies and FPGAs • Weak links between research and industry in memory & storage
• Base new systems on European values and ethical principles to improve security and user-controlled privacy, which is becoming attractive also for other regions • Demand for low power or ultra-low power design. • European demands are or will be really high in terms of security as well as IoT, BT, industry 4.0, smart home applications. • For certain markets we clearly need to rely on European products in memory • Low-resource secure and safe OS framework	• EU unable to keep pace with US and China on AI • Big cloud providers offer integration of (their) services and IoT platforms • Reliance on outside leading-edge processes and FPGAs → Security • Fleets of devices controlled by US and Asia in our premises. • eNVM technology are massively coming from Asia • eNVM design and IPs are coming from both Asia and US
Opportunities	*Threats*

3.1.4.5. Identified key strategic actions

Short term (<2026)
• Develop an MPSoC meta-level description standard for trustworthy integration of third-party IP • Improve existing industrial eNVM • Start industrial transfer of new memory technologies • Develop and research low-resource open OS framework with organizational support for maintaining the system • Plan access to design tools, license costs, IP costs • Set appropriate IPR targets • Reconsider the collaboration and patent strategies in European academia, research institutions, corporations • Establish “digital design kitchens”: parallel innovation of end product and chip platform
Medium term (2026-2030)
• Establish “digital design kitchens”: parallel innovation of end product and chip platform • Support research for low power eNVM for AI • Develop and deploy a modular low-resource secure operating system framework • Involve independent certification bodies to ensure evaluation against European security standards • Confirm the industrial transfer of new memory technologies • Facilitate the transition from the classic memory hierarchy used in von Neumann computers to memory used in emerging non-von-Neumann computers • Invest in 2.5D and 3D packaging

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Long term (>2030)
• Design a new OS-based software stack definition through higher-level abstraction methods • Address research questions related to eNVM improvements • Productize memory technology IP, MPSoCs • Develop and deploy a modular low-resource secure operating system framework

3.1.5. Automotive connectivity

Traditionally, automotive companies were focusing on mechanics. The mechanical units were augmented with sensors and electronic control units (ECUs) that are decoupled from each other. It is expected that these control functions will centralize transforming the car into a full-fledged compute and server platform. The introduction of autonomous driving will further increase this trend towards electronics and software. Wireless connectivity will also play an increasingly important role in new vehicles for over-the-air (OTA) software updates, vehicle-to-anything (V2X) communications, radar technologies and the combination of the latter (joint communications and sensing) [Til21].

Therefore, the "connected" car of tomorrow with positioning and ranging capabilities needs computation platforms that fulfill the following requirements:

- High safety
- High AI performance
- Low latency or even real-time capability.

Such computation platforms are also relevant for other mission-critical consumer devices (e.g., exoskeletons) which may be considered an extension of this market segment.

3.1.5.1. Short term impact (<2026)

To meet the safety requirements given by automotive applications, trust is necessary. Europe should design and develop hardware that enforces trust relations between MPSoC components. This involves safety-enhanced ISAs and an MPSoC meta-level description standard for trustworthy integration of third-party IPs. On the software side, existing European OS frameworks, that already have a strong position and field use in automotive, can be further evolved concerning capabilities and certification efforts for esp. security and safety. Modularity is the key, especially for support of multi-core and many-core systems in safety and security. Both hardware and software need to work together for supporting strong safety and security properties, especially with regards to virtualization capabilities.

AI applications impose high memory requirements that are served best by embedded memories. There are strong research groups in embedding memory in packages, dies, etc. They develop standard interfaces and packaging/integration methods for automotive-grade extendable memory interconnects. The research and development of some memory components are reaching TRL5 in Europe and may be transferred to current products.

3.1.5.2. Medium term impact (2026-2030)

AI continuously needs data for training. Since roads and driving styles in Europe are quite different from those outside Europe, Europe-specific datasets can be collected and made available to European AI companies to gain advantage over non-European companies and remove dependencies from them. With regulations, Europe can ensure that the dataset collection is done in a privacy-respecting manner by integrating Europe-specific privacy

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regulation into components. For example, the system could already blur recorded faces close to the camera sensor before the data is sent and stored.

Novel memory options are under massive development to improve technology maturity leading to better automotive-qualified embedded read-only memory (ROM)/Flash-replacement (eNVM) with high density, endurance, scalability and integrability (on-chip or in-package). AI processing may be enhanced further by the introduction, development, and integration of additional memory features like in-memory computing (e.g., secure memory operations) and self-healing. These are future topics currently addressed by Europe scientists.

3.1.5.3. Long term impact (>2030)

Because of its strong OS capabilities and with continuous efforts, Europe may be able to provide complete base-level OS solutions (no UI) and offer it as a world-wide leading platform for automotive use-cases. As a result, European OEMs gain independence from non-European suppliers.

Europe will establish future fabs locally, thus SoC and novel integration can be guaranteed to be implemented in Europe. Interesting technologies are interchangeable and extendable memory cell in a system-in-package (SiP, 2.5D) or 3D stack to address supply availability and various specifications, supporting rapid design and development.

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3.1.5.4. European strategic position and potential - SWOT

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• Strong automotive industry in Europe • Strong OS position for automotive today, in-field use today • Strong sensor and sensor processing position • Europe is good at power electronics • Strong research activities in the field of novel memory options in Europe	• Europe's approach esp. to safety, security and regulation compared to world-wide competitors too slow • European OEMs have additional burden of transitioning to electric drivetrains • No design house for AI and AI engine accelerators • No infrastructure for GDPR-compliant data set collection • Silo research groups in the field of memory technology
• World-wide leading platform for automotive systems. • Unique compute unit within the car: MPSoC with cloud connectivity • Europe-specific privacy regulations integrated into components and dataset collection infrastructure. • Autonomous driving requires high security and trustworthiness • Collect Europe-specific datasets and make them available to European AI companies • Join force with EU fabs in developing memory options	• European automotive industry moving too slow • Softwarization puts established processes in car companies at risk
Opportunities	*Threats*

3.1.5.5. Identified key strategic actions

Short term (<2026)

- Support development of open modular microkernel-based OS, that can be used in safety and security contexts
- Develop an MPSoC meta-level description standard for trustworthy integration of third-party IP
- Improve existing automotive eNVM
- Start industrial transfer of new memory technologies
- Plan access to design tools, license costs, IP costs
- Set appropriate IPR targets
- Reconsider the collaboration and patent strategies in European academia, research institutions, corporations

Medium term (2026-2030)

- Support research for low power eNVM for AI
- Develop and deploy an open modular microkernel-based OS, that can be used in safety and security contexts
- Involve independent certification bodies to ensure evaluation against European security standards
- Confirm the industrial transfer of new memory technologies
- Facilitate the transition from the classic memory hierarchy used in von Neumann computers to memory used in emerging non-von-Neumann computers
- Invest in 2.5D and 3D packaging
- Collect Europe-specific datasets for AI training with components that have privacy regulations integrated

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Long term (>2030)
• Provide strong common OS and virtualization platform for use in automotive and similar targeted markets, allowing OEMs to concentrate on differentiating aspects of their software platform. Align with hardware vendors for best efficient HW/SW interaction • Address research questions related to eNVM improvements • Productize memory technology IP, MPSoCs

3.1.6. Research areas

In section 3.1.6.1, we will begin with a description of the system requirements for the RAN and the UE (User Equipment) use cases. From these requirements we derive the form needed to fulfill the specific functions at each layer of the computing platform from the bottom-up in this whole chapter (c.f. Figure 12). At the bottom there are the process technologies that are used for physical realization. Section 3.1.6.2 states some initial thoughts on the requirements. Modern computing platforms contain at least one, more often multiple, cores whose software interface is defined by the instruction set architecture (ISA). For different situations, such as infrastructure equipment or edge devices, different ISAs may be used, as elaborated in section 3.1.6.3. The next section, section 3.1.6.4, analyzes the European position in memory and storage and how it can be improved. The challenge of integrating multiple heterogenous cores, memories, accelerators (c.f. EG3) and intellectual property (IP) blocks in a Multiprocessor system on a chip (MPSOC) is portrayed in section 3.1.6.5. Finally, section 3.1.6.6 proposes an operating system framework which is based on the principles of modularity and microkernel architecture.

3.1.6.1. 5G/6G System architecture

The 5G/6G System Architecture is discussed in two parts: first the Radio Access Network (RAN) and next the User Equipment (UE).

The RAN compute platform likely is to comprise multiple System-on-Chips (SoC). These SoCs are realized in advanced CMOS, possibly including new nanoelectronics technologies such as MRAM, and are connected using novel packaging and interconnect technologies.

- Each SoC includes multiple (100s), diverse compute cores. The HW architecture is heterogeneous.
- Cost pressure and the need for software upgrades will push for programmable ISA-based cores, whereas power constraints will dictate a significant degree of specialization, using a variety of specialized accelerators.
- These cores must be real-time capable to support their dynamic allocation on µsec-msec time scales.
- The memory organization will be a key challenge: the need for low cost and high flexibility will push for memory unification and centralization, whereas the need for low power will push for memory specialization and distribution.
- The mix of cores and the memory organization must be such that the overall multi-MPSoC RAN can be scaled over a range of workload sizes.
- Also, new system architecture design and thermal-aware and energy-aware optimization methodologies need to be created to enable trade-offs between security, power and performance for the 5G/6G context.

3.1.6.1.1. RAN run-time mapping

Running the complex, highly dynamic petaflops workload on such a multi-SoC RAN computing platform *efficiently* is exceptionally challenging. It involves:

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- Dynamic, real-time multi-tasking. *Virtualization* is an ultimate form of this, and it is seen as the holy grail.
- Adaptive resource management, meeting power and thermal constraints during operation.

3.1.6.1.2. UE

On the UE side, the main challenges arise from the huge *diversity* in 5G/6G modem requirements, from primitive IoT devices to high-end smartphones. This diversity is about:

- the range of standards (4G, 5G, Wi-Fi, Bluetooth, GPS, NFC, Ethernet…) to be supported,
- the ranges of required bitrates (kbps – Gbps), and latency requirements.

Accordingly, the main architectural challenge is building a scalable modem (as IP block, incl. HW/FW/SW), addressing multiple market segments.

Additional UE architecture challenges include:

- perform MIMO signal processing, support of beamforming, including distributed (coordinated) beamforming by multiple IoT devices
- additional flexibility on MPSoC to enable ISA extensions and use programmable or reconfigurable (coarse-grained or fine-grained) accelerators
- adaptive resource management approaches at system level, including power and thermal constraints at run-time during operation
- potential definition of dynamic, and real-time multi-tasking and architectural flexibility, where virtualization can be an ultimate form of such a flexibility

3.1.6.2. Process technology

The future perspective of programmable computing platforms (PCP) for communications dictates the availability of semiconductor technologies with very specific characteristics. Due to, in many cases, contrary requirements of the components in such PCPs, we can already see today that those computing platforms will consist of components based on application-optimized technologies. Within the digital domain, following criteria will dominate, based on PCP requirements:

- processing speed → computational performance at low power
  - leading edge (7 nm-5 nm-3 nm)
  - thermally optimized 2.5D / 3D packaging technology
- bandwidth → RF semiconductor technologies with peak frequencies above 600 GHz
- real-time → latency → specialized hardware-based AI accelerators
  - low-power technologies for AI on value added technologies
  - low-power embedded Non-Volatile Memory (eNVM)
- cost → cost efficient and reliable 3D packaging technology for system-in-package
- trust → hardware (technology) based secure components (PUFs, secure NVM, etc.)
- sustainable → energy-efficient production and operation

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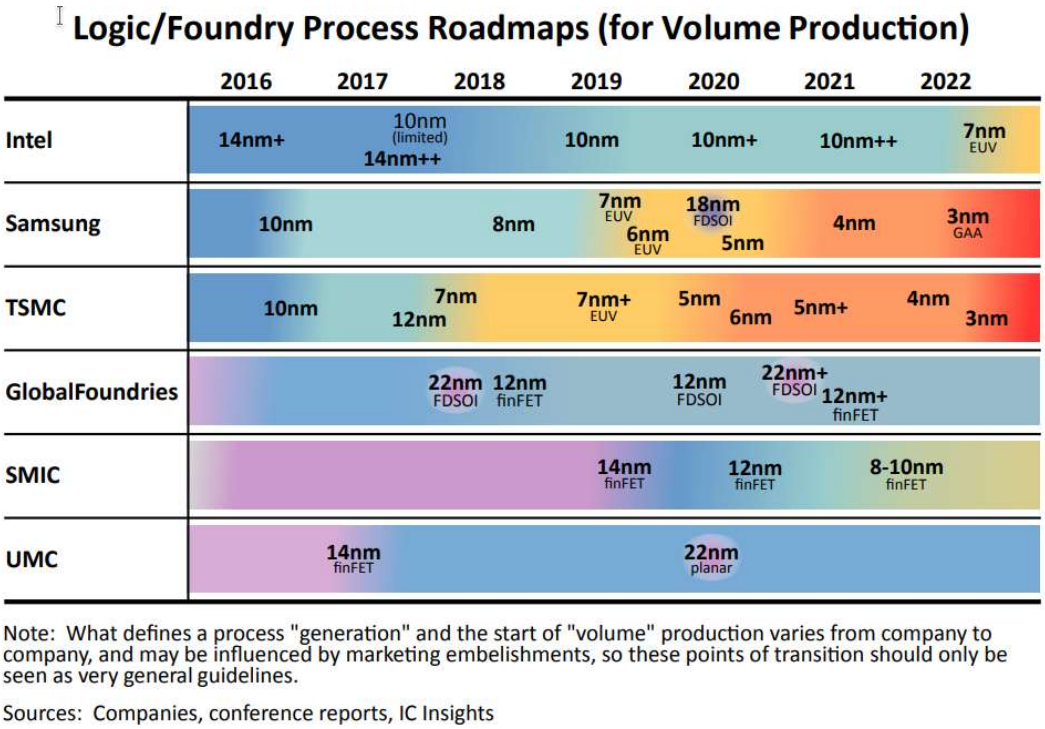

Figure 14: Leading Edge foundry process roadmap [ICI21].

Moore's Law has always been about silicon area, performance, and cost. Continuously increasing amounts of data being transferred and processed will require system components in a PCP which are built based on leading-edge digital technologies ("7 nm", "5 nm" down to "2 nm"). When neglecting the market conditions and the non-recurring costs, these technologies might be capable to resolve the trade-off between computational performance and silicon area cost. Figure 14 shows an overview of the logic/foundry process roadmaps as distributed by [ICI21].

It should be noted that Figure 14 depicts the leading-edge offerings only. Integration of NVM, analog, power and RF into CMOS-technologies can only be done on legacy technologies. This aspect is of high importance, as significant reductions in performance, construction size and cost can only be achieved with deeply scaled integration.

In addition to technology scaling, significant reductions in power consumption can be achieved using specialized AI components performing dedicated tasks within a PCP. These AI accelerators not only contribute to the real-time capability of the entire system. Properly designed and using AI-optimized technology components, like low-power analogue calculators and low-power embedded NVM, these AI accelerators significantly reduce system power consumption. Neither the AI functions, nor the eNVM components require deeply scaled technologies but would like to use the functional integration of moderately scaled technologies. Moreover, eNVM can only be offered in rather mature technologies, which are also available through European semiconductor manufacturers. So, the focus here must be placed more on the architecture and design of such AI components and the usage on trusted technologies from Europe in view to achieve increased sovereignty. In addition, the number of specialized AI accelerators in the PCP should be increased to a possible maximum to save as much power as possible.

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Replacing generic AI-accelerators with dedicated AI-accelerators in deeply scaled technologies, trustworthy and secure provision from Europe, could position Europe well for the future in the context of 6G.

Due to numerous functional components in a future PCP, special focus must be put on the system integration. 2.5D and 3D packaging technology can be used to reduce parasitic limitations (I/O loadings) and thus increase system efficiency to both power consumption and data throughput. On top, appropriate packaging technologies are capable to combine trusted components (AI, eNVM, RF) with those originating from untrusted manufacturing sources (digital "7 nm", "5 nm" down to "2 nm"). Using appropriate components providing trust, untrusted system components can be used and "upgraded" to the required trust level. Unfortunately, standard packaging technologies are not very well represented in the European technology landscape. However, there is the opportunity to gain a lead in advanced 2.5D and 3D integration. Special focus will have to be placed on thermal aspects and we may have to divert some of the gains of Moore's law from "performance" to "lowering power", more than we have done in the past.

Controlling 3D integration will provide us with a lead in designing security solutions and build trusted systems out of Europe independently.

3.1.6.3. Instruction set architecture (ISA)

The Instruction Set Architecture (ISA) and its realization as a microarchitecture can be an enabling factor for innovation as described in D3.1. In the context of 5G/6G applications, we need to consider solutions covering IoT and edge devices as well as infrastructure equipment. For infrastructure equipment standard ISAs provide a good solution, while for small IoT and edge devices more application-specific solutions based on non-standard ISAs/DSLs are needed. For both scenarios also, solutions based on application-specific adaptations of standard ISAs, such as RISC-V which is an open-source initiative for core processor architecture design, play an important role. We identified the following open challenges and topics for each of them.

Standard ISA for infrastructure equipment:

- **High Performance Chip Design:** High performance implementations in silicon are very challenging and require highly skilled CPU architects/designers (and possibly custom design at the gate level), which is currently a scarce resource in Europe.
- **Dynamic Binary Translation (DBT):** Another road to high-performance ISA implementation is using DBT to a simpler core, as done by NVIDIA with the Denver/Denver2 cores implementing ARMv8 ISA and by Apple with the Rosetta DBT. An extended RISC-V implementation could be the target of a DBT, both could possibly be in the EU skillset.
- **Adaptations of Standard ISAs (e.g., 64-bit RISC-V):** There are a few EU 64-bit RISC-V implementations: The Ariane-based from ETHZ (now on openhwgroup.org/cva6), the NOEL-V from Cobham Gaisler, the Avispado and Atrevido from SemiDynamics. It is not expected that EU-designed RISC-V processors become competitive with high-end X86 or ARMv8 implementations in USA or Asia (China, Japan, Korea) for latency-constrained applications. However, it is expected that these eventual performance limitations of EU RV64G cores will not be a major problem for accelerated computing scenarios at the edge, for 5G/6G applications. On the contrary, the ISA adaptation opportunities of the RISC-V environment will enable more tuning for these accelerated computing scenarios, in the privileged ISA (on the memory models).

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- **Formal verification of ISA implementations**: Whether RISC-V related or not (OneSpin also did it on the Infineon TriCore2, on Bosch DSPs, etc.) are of high importance to ensure trustable and reliable realizations.

Non-standard ISAs / DSLs for edge devices:

- **Non-standard ISAs:** Can be hidden and easily integrated into the software stack if they operate beyond a DSL; this is already the case for AI in Multi-access Edge Computing and could be the case for the L1/L2 RAN processing.
- **Acceleration DSLs:** May lead to specific/relaxed requirements on the accelerator memory model and the way it is seen from the GPP. Having the accelerator to operate under CAPI, CCIX or CXL may be less important than in datacenters, as latency and energy-efficiency plays a crucial role in the edge.

3.1.6.4. Memory and Storage

In this section, we describe our vision of Europe's industry roadmap in the broad field of storage, including on-chip memory. First, we discuss the scope of this roadmap. Second, we perform a situation analysis by addressing the following questions:

- Why is it important for Europe to work on storage?
- In terms of storage, what are the key developments and trends inside and outside Europe?
- In terms of storage, what is Europe's wanted position in 10 years?

Third, we discuss industry targets for Europe in terms of storage during the next 10 years to be able to reach the wanted position. Fourth, we discuss research questions that Europe should address to be able to meet these industry targets. And finally, we discuss partners and competences that Europe would need to be able to conduct that research and reach the targets.

3.1.6.4.1. Roadmap Scope

The scope of this roadmap can be described as follows. The main scope is on the architecture level of the on-chip memory hierarchy, including:

- new packaging technologies (e.g., 3-D integration, chiplets, large-scale wafer)
- on-chip memory interfaces and interconnects
- embedded non-volatile memory (eNVM) and especially low-power eNVM
- high-bandwidth DRAM (HBM DRAM)
- intellectual property (IP) for on-chip support of wireless storage (storage-over-radio-network) enabled by low-latency and high-bandwidth connectivity like 5G and 6G

The scope does not include, e.g.:

- off-chip DRAM DIMMs
- memory-technology details like materials and device physics

We discuss embedded technology access only in cases where we can strongly motivate its strategic weight for Europe.

3.1.6.4.2. Situation Analysis

The first question of the situation analysis is: *Why is it important for Europe to work on storage?* Today there are no companies in Europe that work on storage, and this gap is a potential threat to Europe. By working on storage, Europe can *understand* the design of memory IP and thus be

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able to do memory-aware system design (i.e., acquire competence to design systems-on-chip (SoCs) and systems-in-package (SiPs) that have efficient utilization of the memory hardware). Further, Europe could *master* the design of memory IP (including circuit design) and license that memory IP to the rest of the world.

The second question of the situation analysis is: *What are the key developments and trends with respect to storage inside and outside Europe?* We would like to point out that memory research in Europe is manufactured outside Europe. At the same time, Europe imports memory components. [Kle21] claims that fabs are decreasing in their numbers and provide to external parties less and less access to design kits and technology details of their memory IPs. As such, Europe needs to assess the potential threat of this evolution. Another trend is that technology giants outside Europe prefer to either master technology themselves or to acquire European companies that own the technology. This means that it might become more difficult for Europe to benefit from licensing memory IP. Another trend is that due to miniaturization and higher integration, memory and storage converge. This means that 3-D integration might be a key technology. At the same time, we know that data amounts grow faster than local (on-device) storage capacity, which increases the usage of wireless storage (e.g., storage-over-radio-network, such as cloud accessed via a cellular network).

The third question of the situation analysis is: *What is Europe's wanted position with respect to storage in 10 years?* We think that Europe might want to master 3-D integration – a technology on which other countries might depend. Europe should be able to affect standardization in councils like JEDEC, where Ericsson and Nokia are members. Europe can have strong bonds with strategic partners cleared by governments to minimize the risk of supply chain disruptions due to factors like trade wars. Since Europe has Ericsson and Nokia, Europe can use this momentum to further increase the use of such wireless storage. We think that Europe must be able to research and innovate (R&I) *at least* on the architecture level and to productize systems (i.e., to be able to design SoCs that employ innovative memory IP and then productize such SoCs). A higher level of ambition for Europe would be to also R&I on the memory-component design level and to productize components. Like we mentioned in the description of the scope of this roadmap, embedded technology access requires strong motivation, and here we merely describe it as the highest ambition level for Europe's wanted position.

3.1.6.4.3. Industry Targets

Regarding industry targets for Europe with respect to storage during the next 10 years, we have the following recommendations. In general, we think that Europe needs to increase the amount of collaboration among European entities (currently, there are more collaborations with entities outside Europe). Such collaborations include knowledge exchange between academia, research institutions, and corporations. To increase such collaborations, Europe should reconsider the collaboration and patent strategies in European academia, research institutions, and corporations. To keep momentum in standardization, Europe should set appropriate targets in increasing the European portfolio of IP (e.g., patents) in the broad field of storage, even if European companies do not productize such IPs.

In terms of work on disruptive technologies, Europe could consider facilitating the transition from the classic memory hierarchy used in von-Neumann computers to memory used in emerging non-von-Neumann computers. In terms of securing leadership, Europe could focus on

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3-D integration, as the technology is still relatively new, yet it has a potential of becoming a future dominator technology.

3.1.6.4.4. Research Questions

Regarding research questions that Europe should address to reach its storage-related industry targets during the next 10 years, we recommend choosing an appropriate level of ambition (architecture level, circuit-design level, or technology level). On the architecture level, we consider questions about:

- SoC design
- chiplet library
- 3-D integration
- integration of eNVM for high-density on-chip storage
- tight coupling of SRAM and eNVM
- hybrid memories like eDRAM & eNVM
- efficient integration of storage-over-radio-network into the memory hierarchy

On the circuit design level, we consider questions about:

- memory throughput (e.g., pipelining)
- memory interfaces (e.g., vectorization)
- latency / bandwidth / energy optimizations of components used in storage-over-radio-network
- the support of multi-level cell (MLC) operation (e.g., programming and sensing techniques)

On the technology level, we consider questions about eNVM improvements, e.g.,

- how to increase endurance
- how to reduce cell variance and thus enable MLC with greater numbers of logical levels
- how to reduce operational latencies
- how to reduce power
- how to reduce the process node and thus mitigate the dependency that eNVM might limit the process node for the rest of the chip

3.1.6.4.5. Partners and Competences

While Europe lacks an industrial leader in Memories, some partnerships might be established to feed this strategic area:

- on the architecture level: Bosch, Dolphin Design, Ericsson, Infineon, NXP, ST, Nokia
- on the design level: Fraunhofer, imec, CEA, Siemens EDA
- on the technology level: ST

Outside Europe, potential partners are:

- on the architecture level: Apple, Intel, Kioxia, Micron, Qualcomm, Renesas, Samsung, SK Hynix, Western Digital
- on the design level: ARM, Intel, Synopsys, TSMC
- on the technology level: GF, Intel, Samsung, SMIC, TSMC

3.1.6.5. Multiprocessor system on a chip (MPSoC)

Besides considering the initial requirements regarding trustable blocks, and security indicated in D3.1, which all are key research questions for the MPSoC level in the three scenarios shown in section 0, the core concept that needs to be developed at the MPSoC level is the definition of

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a new meta-level description standard. This new standard needs to provide common interfacing between IP blocks and units of the MPSoC to operate in real-time during run-time operation. Moreover, this standard must guarantee real-time scheduling (microsecond level) in close coordination with the OS level.

As a result, we have identified the following five core challenges and topics to cover in the design of MPSoC for the 5G/6G context to develop the aforementioned core concept:

- New MPSoC design and optimization methodologies need to be created to enable trade-offs between security, power consumption, performance, and time-predictability in the 5G/6G context. MPSoC design is not currently real-time capable (i.e., it can fulfill hard-real time of ten µsec to few msecs latency). Therefore, to accommodate this requirement today, MPSoCs used in telecom infrastructure are massively over-provisioning the memory hierarchy (power and area wastage).
- Additional flexibility on MPSoC to enable ISA extensions and use programmable or reconfigurable (coarse-grained or fine-grained) accelerators for the compute-intensive parts of 5G/6G layers. Currently, the key elements or blocks used in this context by industrial designs are hard-coded IP hardware accelerators or FPGA devices. However, the latest communication standards need to be more flexible to enable scalable MPSoCs to increase system performance by including more specialized processors, AI chips to increase automation and heavily heterogeneous designs.
- Hardware/Software co-design of MPSoCs for the 5G/6G context requires a new higher-level software stack definition. This part must include the OS and development frameworks to exploit further application-level knowledge to understand the performance bottlenecks of different 5G/6G services and effects on the MPSoC architectural blocks. In this context, the classic use of coordination languages based on execution models, such as dataflows, is not enough. These languages are too rigid to adapt to the time-varying nature of telecommunications workloads.
- A new generation of flexible interconnects for MPSoCs needs to be added to system components and IP cores that support the real-time capabilities. In particular, these new interconnects should enable terminating and activating the macro network interfaces, such as synchronized or time-sensitive Ethernet, in the elements of the MPSoC architecture. In this context, this new generation of MPSoC interconnects has to ensure the quality of services, including guaranteed latencies and throughput.
- Definition of how to interconnect multiple MPSoCs as beamforming and other operations of 5G/6G require multiple MPSoC instances to cooperate and operate synchronously closely. Therefore, new connection standards needed for 5G/6G at the MPSoC level require to go beyond near-memory standards or classical networking interfaces to get more efficiency. In addition, at the MPSoC level, it is necessary to control functional isolation and security for the distributed infrastructure.

3.1.6.6. Operating System Framework

The Operating System Framework is the common ground for the base-level software platform that facilitates all use-cases targeted by COREnect, and beyond. All use-cases have in common that any network-connected system needs a sound base-level software platform that can fulfil indisputable requirements of security, safety, and trustworthiness, together with versatility, real-time, virtualization and applicability to run multiple distrusting applications with diverse and potentially contradicting requirements on a single platform. The framework shall also closely follow and collaborate with hardware development for an efficient interaction between software and hardware.

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COREnect addresses the areas of mobile devices, infrastructure, e.g., cloud and HPC, as well as severely constrained devices used in sensors and IoT applications, which is a wide range of the hardware and compute scale. Further, ongoing development in the hardware area pushes the increase of compute capacity and overall resources by adding more cores, increasing interconnect bandwidth, and adding diverse compute units (commonly called accelerators). All this is driven by the mobile and cloud markets that have a high volume and consequently resources to invest into the evolution of IT hardware architectures. On the software-level, this evolution cannot be observed. Currently, there is no base-level operating system software implementation that can address the increasing demand on the hardware and its diversification due to accelerators and the difficulties to continue with Moore's Law.

Given the wide range of hardware and different applications that shall be covered, there is no "one size fits all" approach to design an operating (OS) system. The OS rather needs to be a modular system that can provide the required functionality in both features and properties such as security and safety and fully exploit the functionality of modern and future MPSoCs. Modularity enables that only functionality is included that is required, leaving out unnecessary software complexity, and allows to cluster functionality. Thereby the system can be built with multiple isolated domains. A generic OS is therefore actually a framework of building blocks, allowing to build application-specific systems and subsystems within one system such that all requirements, especially for safety and security, can be implemented. The key ability is to minimize dependencies as much as possible such that only required functionality is within the dependency of a feature. Eventually the framework allows to build, together with virtualization technology, a hierarchy of operating systems running on the base-level OS.

Modularity is also becoming a cornerstone to the base-level software as architectures are getting more distributed by placing compute units across a platform. Distinct computing systems are not only running in the general-purpose CPUs but also in peripherals and devices, e.g., in Smart-NICs/DPUs, as well as in computing systems that are connected to the same memory or are connected via fast coherent or non-coherent connections or networks, such as CXL, CCIX, or Gen-Z.

COREnect therefore recommends that an operating system framework follows an architecture that is based on an open microkernel design, which is founded on modularity from the ground up and passes the following distinct criteria:

- A modular, microkernel-based system that focuses on security, safety, reliability, and trustworthiness: Only with small software modules it is possible to implement convincing security, safety, and real-time properties that can eventually withstand evaluation and certification as required for many important use-cases.
- Modularity also brings flexibility in system design and consequently portability and adaptability to different use-cases and upcoming hardware evolutions.
- Openness is required to establish trustworthiness of the system, allowing an independent evaluation of it. The best approach to providing the required openness is an open-source system.
- The OS software layer needs to be efficient to provide applications as much compute resources and thus minimize power consumption. Providing necessary means for controlling hardware regarding power consumption is a must.
- For a broad applicability, the OS needs a decent level of documentation and accompanying documentation such that it is generally usable.

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- The system needs to provide a decent level of compatibility to be able to host existing software and applications which is typically implemented through virtualization techniques and providing common APIs for applications.

Europe is in a distinct position for an open and versatile operating system framework with prior research and development that went into secure, safe, real-time, and open-source operating system designs and implementations, funded by EC and national funding bodies. Ideas and implementations have been brought out of academia and are used in industry for selected use-cases today. Building upon those initial research and funding investments as well as industry experience, we propose that an operating system framework shall be developed openly and collaboratively for the benefit of providing an open and accessible OS framework. This shall avoid parallel development efforts and multiple, possibly incompatible, implementations for the benefit of all.

Providing an open, secure, and safe implementation of a versatile operating system framework on common hardware platforms, developed together with ongoing hardware activities, requires support and resources. Besides the core development and maintenance, especially providing the necessary means for qualified software demanded by many markets, needs support and resources as the required efforts are substantial for achieving the high level of confidence required for software.

3.1.7. Recommended actions for compute and storage

In conclusion of our analysis, we recommend the following key strategic actions that are relevant for all or most market segments and research areas. The short-term actions are mostly focused on IP development, patents, and regulations and on basic research. As a result of these efforts, solutions are designed in the medium term and in the long term productized and sold.

Short term (<2026)
• Ensure activity in JEDEC and PCI-SIG • Protect European patents in computing and storage • Foster digitization of European industries • Secure access to < 7 nm CMOS technology • Develop RISC-V ISA extensions to enable inclusion of programmable accelerators • Improve existing European eNVM • Start industrial transfer of new memory technologies • Plan access to design tools, license costs, IP costs • Set appropriate IPR targets • Reconsider the collaboration and patent strategies in European academia, research institutions, corporations • Develop an MPSoC meta-level description standard for trustworthy integration of third-party IP • Support development of open modular microkernel-based OS, that can be used in safety and security contexts

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Medium term (2026-2030)
• Collect and organize access to Europe-specific datasets for AI training with components that have privacy regulations integrated • Establish “digital design kitchens”: parallel innovation of end product and chip platform • Push for isolation mechanisms for sensitive pieces of data in the 6G standard • Invest in 2.5D and 3D packaging • Encourage the industrial transfer of new memory technologies • Facilitate the transition from the classic memory hierarchy used in von Neumann computers to memory used in emerging non-von-Neumann computers • Push for open accessible hardware platforms and low-level system stacks to enable replacing individual components with European-grown alternatives • Develop and deploy a modular microkernel-based secure OS framework, European cloud and hypervisor technology • Involve independent certification bodies to ensure evaluation of OS against European security and privacy standards
Long term (>2030)
• Establish leading-edge technology source in Europe • Address research questions related to eNVM improvements • Productize memory technology IP, MPSoCs • Design a new OS-based software stack definition through higher-level abstraction methods

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3.2. EG2: connect and communicate

Wireless communication is gradually plays am increasing large role in our lives. While today the first wave of 5G is gradually being rolled out, with the later generations of 5G and certainly 6G wireless communication will become present in any aspect of human and machine interactions. While first 5G applications operate in the frequency spectrum below 10 GHz, the so-called FR1 band (410 MHz – 7.125 GHz), the FR2 band (24.25 GHz – 52.6 GHz) will be used later for very high data rate capabilities over short ranges. The timing of the deployment can be different for each region, and it will depend on the level of saturation in the usage of lower-frequency bands. In a later phase of 5G, the FR4 band (52.6 GHz - 71 GHz) will be used. While first 5G products are or will soon be available, the roadmap described in this document targets the next generation 5G products and certainly 6G.

The broad deployment of wireless communication challenges the supporting connectivity infrastructure. This domain is a very important one for Europe as it has several key players in the supply chain of this infrastructure. Capacity will have to grow here, inevitably leading to the need of faster electronics in the transceivers.

Different domains

For the roadmap discussion in this section, we divide the field of “connect and communicate” into the following domains:

- Connectivity infrastructure:
  - Radio access networks (RAN)
  - Wired infrastructure (datacenters, optical network)
- Consumer grade connectivity
- Industrial grade connectivity

The domain of Automotive connectivity, as outlined in the introduction of Section 3, is not treated here in a separate section. The reason is that concerning wireless communication to and from a car (V2X, V2V), the car can be seen as a “mobile” terminal, as it is the case with a phone, a tablet, ... Speed is different, latency is crucial, data rates are similar, and we can consider that connectivity to the infrastructure is similar with, however, some specific properties.

Transceivers

The generic block diagram of a wireless or wireline transceiver is shown in Figure 15. In between the transmit part and a receiver (from another transceiver elsewhere), there is a medium, which can be the air, a cable, a PCB track, ... The interface from the electronics to the medium is either an antenna or antenna array for wireless communication, a photodiode for optical wireline communication and a copper wire for other wireline communication. The analog electronics make the connection between the digital part of a transceiver and the interface to the outside world. In between the analog electronics and the digital part, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) perform the conversion from the analog to the digital domain or vice versa. The functionality of the analog electronics depends on how much functionality of a classical analog front-end is implemented in the digital domain. There is a shift towards the digital domain of functionality that is classically performed in the analog domain. Examples are seen in digital transmitters for wireless communication and in highly digital wireline transceivers.

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Figure 15: Generic block diagram of a transceiver.

In this section, we refer to the **microwave frequency region** as the region of carrier frequencies roughly below 20 GHz, whereas we call the **mm-wave region** the frequency band above 20 GHz up to 100 GHz. Above 100 GHz we address the spectrum as the **sub-THz band**.

Microwave frequency region

A large part of this roadmap stresses mainly mm-Wave opportunities and non-CMOS technologies, but the timing of adopting the mm-wave frequency spectrum on a large scale is not fixed. Indeed, if new spectrum below the mm-wave frequency is opened for cellular companies to use, it will be exploited prior to a move to the mm-wave region. This also means that innovation is still needed in the microwave frequency region. In this frequency region it is probably an illusion to let Europe take up a role in transceiver and digital baseband design for the consumer market, but there is still a role for Europe in the wireless infrastructure market and the industrial grade connectivity market. Strong investments in low-GHz CMOS mixed analog-digital architectural innovations are key to be successful in any connectivity market. Further innovations in design re-use by focusing on flexibility are key (software defined MIMO transceivers). Moreover, combining flexibility with energy efficiency remains a key challenge and a market opportunity. Maybe O-RAN (Open RAN) developments (see also Section 3.2.1.1.1.2) and industrial connectivity opportunities can have interesting overlaps in mixed-signal processing and software defined transceiver hardware. Multi-market hardware may also be of interest to the European defense industry, where chip development is often not affordable given small production series.

Millimeter-wave region and the sub-THz band

The quest for more bandwidth has led to the allocation of frequency bands entering the mm-wave frequency region. With the advent of 5G, the lower part of the mm-wave spectrum is being/will be used for wireless communication first for wireless backhaul and later for the consumer market. 5G will first use the so-called FR2 band (parts of 24.25-52.6 GHz). In the spectrum around 60 GHz will be used later in 5G: while this was initially limited to the freely available spectrum between 57 GHz and 64 GHz, it is now extended to 71 GHz, and this part of the spectrum is referred to as the FR4 band.

6G wireless communication will make use of frequency bands from 5G and its predecessors but in addition use extra bands. A clear extension of the spectrum beyond 5G is the use of carrier frequencies above 100 GHz, which we address here as (sub-)THz communication. Here, the D-band will be used initially. There are two definitions of the spectrum of the D-band: the waveguide D-band is from 110 GHz to 170 GHz, while the ETSI Industry Specification Group (ISG) on mm-wave transmission (mWT) defines the D-band from 130 GHz to 174.8 GHz. In a later phase, even higher frequencies than the D-band can be addressed (e.g., the first standardization efforts have resulted in IEEE 802.15.3d, which targets the spectrum 253–322 GHz, which is the higher part of the G-band). However, a lot of communication in 6G, if not the majority, will

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happen below 100 GHz, using existing frequency bands or gaps in the microwave and mm-wave spectrum.

The broad deployment of wireless communication so far has only been possible thanks to the downscaling of CMOS, which came along with a speed increase of the devices. However, transistor speed, expressed in terms of the maximum frequency oscillation f_{MAX}, at which power gain has dropped to 0 dB, is saturating to a value below 400 GHz for downscaling beyond the 28 nm generation. This means, for example, that in the D-band (roughly at one third of this 400 GHz) the maximum power gain per stage has a theoretical maximum of 3. However, in practice it is always lower due to losses in passive components. Further downscaling of CMOS does not boost f_{MAX} anymore, it only leads to a reduction of the size of digital standard cells, still giving a performance and area improvement for digital signal processing but not anymore for analog signal processing at high frequencies.

Sustainable radio communication

The expected demand for even more wireless data communication can only be sustainable if the energy consumption of this equipment is kept sufficiently low. This is a challenge for the digital baseband electronics: efficient algorithms, the use of machine learning and AI and the use of advanced CMOS will be required. For the analog transceiver, the high frequency of operation is challenging when energy consumption has to be minimized, especially when the spectrum reaches out to mm-wave and sub-THz frequencies. CMOS has its limitations in speed but also in the efficient generation of transmit power generation. For power generation beyond the limitations of CMOS, a broad set of other technologies are used nowadays: LDMOS, SiGe HBT, GaN, GaAs, InP, depending on cost and form factor requirements, transmit power and frequency range. Communication systems needed to realize the scenario described in the vision, will then consist of a CMOS part for the complex operations both in the digital domain and in the analog domain, while the parts that go beyond speed and/or power capabilities of CMOS use non-CMOS active devices. This inevitably leads to a heterogeneous system for which the integration in a 2D, 2.5D or 3D fashion is also challenged for minimal energy consumption.

3.2.1. Connectivity infrastructure

The growth of the number of internet users - both human and machine-type users (IoT) - will be accompanied with a growth of the supporting infrastructure. Also, the amount and the rate of the data exchanged with end users will grow. The exponential growth of the amount of data transported inside data centers can be expected to continue and even accelerate due to increasing reliance on novel software approaches such as AI.

An overview of the infrastructure is given in Figure 16. End users communicate with the Radio Access Network in a wireless fashion. Inside datacenters and central offices, servers and/or racks are connected with each other. Further, there are wired inter-datacenter links and metro networks that connect datacenters and cities and long-haul networks that span continents and cross oceans. Closer to the end user, there are the optical access networks such as passive optical networks (PONs) that support fiber to the home. Finally, data generated by mobile services are carried by specialized fronthaul and backhaul links to the core of the network. In all these links the throughput will grow giving rise to higher data rates. In the wireless part the higher data rates are addressed by using more bandwidth, going to MIMO and using a higher spectral efficiency with more complex modulation schemes. In the wired communication, the

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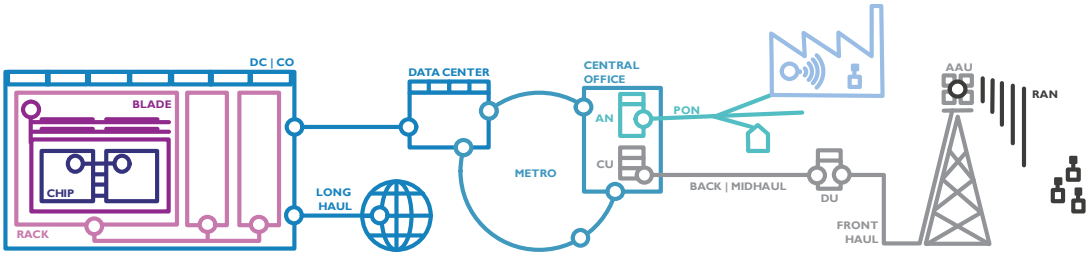
higher data rates are obtained with higher spectral efficiencies, moving from NRZ to PAM-4 and even higher constellations like QAM16 in coherent transceivers.



DC: Data Center
CO: Central office
DU: Distribution Unit

RAN: Radio Access Network
AAU: Active Antenna Unit
PON: Passive Optical Network

Figure 16: simplified view of the communication infrastructure.

3.2.1.1. Wireless infrastructure

The access points that directly interact with the end users will cover a broad range from outdoor to indoor, from large cell to small cells or even without the usage of cells as targeted in cell-free massive MIMO. The number of wireless access points will increase significantly in the coming years due to two evolutions: first, there will be a significant increase of the number of end users both humans and machines. Secondly, when operating frequencies move up, the path loss increases, which necessitates to bring the access points closer to the end users. The consequence of having much more access points will be that the pressure on the energy consumption will be higher for sustainability reasons. As already pointed out in Section 2.3, Europe has a strong position in the wireless infrastructure market and this position should not get lost.

The new RAN will heavily rely on software-defined solutions, meaning that virtualization of the RAN will be essential for new 5G architectures, where the use of software-defined solutions will bring flexibility to the architecture in both terms of functionality (software) and openness (multi-vendor/hardware). Within this future scenario Open RAN aims to improve interoperability in the future network architectures and deployments, in particular when referring to disaggregated multi-vendor solutions. The next section discusses Open RAN more specifically. After these sections, the more hardware-related items are discussed.

3.2.1.1.1. Short-term needs

3.2.1.1.1.1. Fast deployment of 5G

Europe cannot afford to miss the 6G opportunities. R&D focused on the different areas needed for 6G itself is not sufficient. It should be complemented by a quick and broad rollout of 5G over the whole of Europe. This sets the good initial conditions for the European players in 6G hardware and for the European market to efficiently absorb 6G products in a timely manner. Only such climate allows the growth of an ecosystem that is prepared for 6G. Further, a wide and timely deployment of 5G allows to take the learnings 5G into account for 6G.

Meeting the growing demand for broadband connections in households and SMEs will require a deployment of fiber-to-the-home (FTTH) technology. Deployment of that technology is expensive and time consuming due to infrastructure works. An alternative is fixed wireless

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access (FWA) where access points can be installed on roofs or facades of apartments or on light poles. This technology enables a quicker deployment with less drastic infrastructure works.. Also, in rural areas where a wired infrastructure is not available, FWA should be deployed swiftly.

3.2.1.1.1.2. Open RAN

Open RAN aims to create a multi-vendor RAN solution to improve network flexibility, competition and costs. Such solution will enable the functional disaggregation between hardware and software, offering open interfaces via software solutions that controls the network. The current initial deployments based on Open RAN, are exploring –and validating- the impact on performance KPIs (e.g., latency) due to the disaggregation, as well the impact on security. The O-RAN alliance is defining the specifications for the software-based RAN considering the specifications of 3GPP. The O-RAN alliance is an Operator and Vendor oriented organization which aims to provide the specifications and recommendations to enable interoperability among different vendors and to enable new functionality with the support of AI/ML for intelligent control and aims to provide efficient management and orchestration of the RAN.

As mentioned above, there is a strong software component in the new RAN, where hardware needs to be aligned to open RAN to be 'pluggable' in the network and easily orchestrated via the common interfaces. Therefore, hardware needs to be capable to host the flexible open RAN software. In other terms, hardware which is locked to a closed solution will be no longer be interesting for the use of networks operators.

Europe requires to have strong players in the Open RAN ecosystem. The O-RAN alliance comprises the big players (operators and vendors) from the USA, Asia, and Europe. However, there is sufficient room for smaller players (vendors and integrators) that can innovate in the different RAN components from HW and/or SW perspective. European players could strengthen their position in the Open RAN arena from an integrator perspective, where their expertise on the open SW of open RAN is demanded by different worldwide vendors. Moreover, the emergence of the players may be associated not only to open RAN but also to companies with strong hardware (vendors) or software (vendor/integrator) expertise.

As open RAN evolves, other capabilities are expected to emerge and to further develop its capabilities related to intelligent and programmable RAN. This may pave the way for new actors like startups to emerge and take relevant roles. The European Commission, through the launched study on 5G supply markets and Open RAN [Eur20], certainly has included Open RAN in the roadmap of the Digital Strategy for Europe, considering Open RAN as a key technology to be addressed and to be prioritized by European companies (both small/medium and large companies). In the long run, operators must be able to offer connectivity based on flexible, multi-vendor, disaggregated architectures without compromising security, reliability, availability, QoS, and energy efficiency.

3.2.1.1.1.3. Microwave front-end design including RF filtering

The electronics between the transceiver and the antenna/antenna array is termed the front-end. Next to the active circuits (PA, LNA) it typically contains filters, isolators, transmit/receive switches and duplexers and multiplexers.

While in the front-end there is today heavy competition from non-EU companies, the EU still has some major players. The new frequency bands below 10 GHz and the adoption of massive MIMO

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will necessitate the design of new front-end modules on the short term. For the active circuits silicon-based technologies are considered that can go beyond the power capabilities of CMOS (BiCMOS, RF SOI, LDMOS) while RF GaN (see also Section 3.2.1.1.1.6) is pushing away LDMOS for better efficiency and higher frequencies (like upper part in the C-band).

RF filters are needed in the microwave range, especially in the low-GHz range. Indeed, the spectrum is crowded such that a wireless receiver can pick up interferers and jammers, which need to be suppressed early enough in the receive signal path such that these unwanted signals, which can be several orders of magnitude stronger than the wanted signal, do not drive the active circuitry in the receiver into saturation. RF filtering nowadays makes use of off-chip passive components like surface acoustic wave (SAW) filters and bulk acoustic wave (BAW) filters such as FBAR filters. Such filters typically use piezoelectric materials which are often not suitable for manufacturing in a CMOS-compatible processing environment. Recent breakthroughs in Europe, both at industrial level (see [Soi20]) and at research level (see [PiT20]), provide technologies that enable RF filter design and production on a large scale with the prospect of compact heterogeneous integration with active components. Banking on these results is again a means for Europe to play a role in a field where today Far East and USA players are leading.

3.2.1.1.1.4. mm-wave beamforming transceiver and front-end design

At mm-wave frequencies, the path loss, which is the loss between the transmitter and the receiver is considerable. This can be compensated with beamforming (see Figure 17). Whereas mm-wave IC design has been mainly limited to research and solutions for wireless backhaul (E-band) in the era before 5G, the mm-wave frequency bands are going to be massively deployed, provided that the energy consumption per bit is lower compared to the narrower frequency bands used in the microwave region.

Operation at mm-wave frequencies will require extra IC design skills: the transceivers, which contain the electronics to perform the frequency conversion between RF and baseband, will need new functional blocks due to the beamforming. Moreover, the design flow for mm-wave ICs is more complicated than for the microwave region. Indeed, due to the higher sensitivity to electrical parasitics (1fF at 30 GHz is 10x more visible than at 3 GHz), there is a larger influence of the circuit layout on circuit performance. Further, mm-wave IC design requires more EM simulations.

Typically, most of the functionality of a transceiver will be based on (RF) CMOS and BiCMOS. While at the transmit side, beamforming reduces the transmit power per PA for a required total transmit power, still the required transmit power might be too high for CMOS PAs. In that case, a trade-off can be made between the technology for the PA and CMOS for the implementation of the beamforming electronics.

While today the transceiver market is mainly dominated by US players even if the main RAN players (Huawei, Ericsson and Nokia) do develop internal ASIC solutions, the evolution to mm-wave and beamforming is an opportunity for Europe to increase its role in the market of mm-wave ICs for wireless infrastructure. This also implies that European universities and research centers should educate sufficient students and researchers for mm-wave IC design work. This should come together with a climate that eases startups for design houses and fabless companies.

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3.2.1.1.1.5. Towards more digitization in transceivers

The increase of wireless data communication, be it at microwave, mm-wave or sub-THz frequencies, will inevitably lead to higher complexity in the signal processing (e.g., implementation of beamforming, cell-free massive MIMO, ...) and AI will be involved. This high complexity would justify the use of highly downscaled CMOS. Another incentive for the use of highly downscaled CMOS is that the energy consumption is kept within sustainable limits. The exact choice of the CMOS generation, however, requires attention as the non-recurring engineering cost increases with downscaling, while volumes for base stations are small compared to user equipment.

The design of complex base station chips in Europe requires that enough engineers should be available for digital design in advanced CMOS technologies and that European universities and research centers provide sufficient education and training in this domain. Again, it is important to mention here like in section 3.4, that this should come together with a climate that eases startups for design houses and fabless companies. Next to the massive digital part of ICs, the data converters (analog-to-digital and digital-to-analog) most often reside on the same chip as the digital part, and hence, sufficient design skills for data converters need to be present.

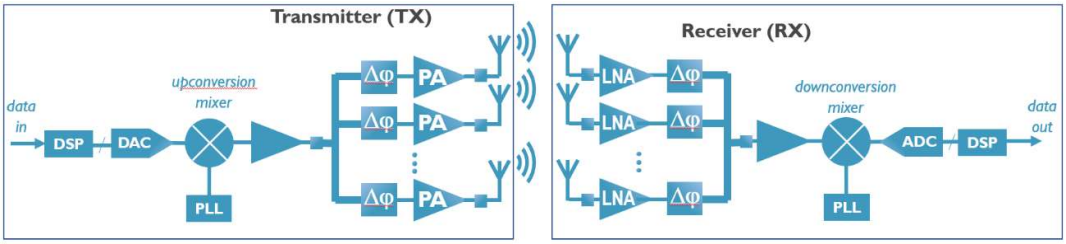

Figure 17: Beamforming in a wireless transceiver (PLL: phase-locked loop, LNA: low-noise amplifier, PA: power amplifier, ADC: analog-to-digital converter, DAC: digital-to-analog converter, DSP: digital signal processing, Δφ: phase shifter).

3.2.1.1.1.6. RF GaN

In wireless communication, generation of transmit power with a sufficiently high efficiency is always a challenge. Base stations operating in the low-GHz range today still use silicon-based technologies such as BiCMOS, LDMOS but it is seen that RF GaN is gaining traction here, pushing away LDMOS for better efficiency and for the higher frequencies. On the short term, the introduction of RF GaN focuses on the low-GHz range. In the medium term, the speed of GaN can be increased by scaling down the gate length. This will be discussed in Section 3.2.1.1.2.1. Whereas (RF) GaN on silicon carbide (SiC) is the most widely used material scheme, certainly for base stations today, GaN on silicon is a cheaper alternative. GaN-on-Si cannot handle as much power as GaN-on-SiC but it could be used for smaller-cell base stations, AAS (Active Antenna System) base stations where each single PA has quite moderate power levels or in general for applications where GaN on SiC is an overkill in terms of performance. According to [Yol21], the total GaN RF market's value reached US$891 million in 2020, while CAGR 2020- 2026 of 18% is expected. Still according to this report, the GaN-based macro/microcell will represent more than 95% of the total GaN telecom infrastructure market in 2026. The 5G telecom infrastructure applications will represent 41% of the entire RF GaN device market by 2026.

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At the foundry level, Europe has various RF GaN foundry players, both at industrial level and at research level. The European RF GaN foundry players should be able to cope with the expected growth of RF GaN and an effective spill-over from research to production is needed.

While RF GaN devices (HEMTs, high-electron-mobility transistors) have the potential of generating higher output powers and are enabling higher efficiency than their silicon counterparts, their nonlinear behavior with memory might limit the spectral efficiency of wireless transceivers. This behavior is probably more pronounced in GaN-on-Si than in GaN-on-SiC. Spectral efficiency can be improved with advanced predistortion techniques that can cope with the memory effects. A successful deployment of RF GaN therefore should come with efficient predistortion solutions. Efficient predistortion techniques require a combination of device modeling, characterization, system, and algorithmic know-how. Here is an opportunity for EU universities and research centers to train sufficient engineers that can move on to the involved industrial players in Europe.

3.2.1.1.1.7. SiGe BiCMOS for microwave and mm-wave transceivers

When it comes to generation of transmit power at microwave and mm-wave frequencies, SiGe BiCMOS HBTs can generate more RF transmit power than CMOS and with a higher efficiency. Moreover, for the same fT and fMAX of a SiGe HBT and an nMOS device from a CMOS process, BiCMOS wafers are cheaper than CMOS ones. SiGe BiCMOS is used today in base station chips from the low-GHz to the mm-wave frequency range. European foundries are in a strong position regarding BiCMOS SiGe processes, either in industrial or research organizations such as ST, Infineon, NXP, and IHP with strong academic teams. Continuous improvement of the SiGe HBT fT and fMAX is fundamental for next-generation BiCMOS process platforms, to get the needed design margin for product performance robustness and to well exploit the unique feature to integrate the digital and analog functionalities locally in each active channel of an antenna array. In contrast with a MOS transistor, the speed of a SiGe HBT transistor is not yet saturating. Predictions have indicated that fMAX can go beyond 1 THz (but at a lower breakdown voltage than an InP HBT).

3.2.1.1.1.8. Heterogeneous integration of transceivers

The functionality of a transceiver will be realized with digital chiplets, and analog transceiver and front-end circuits, potentially using different technologies. With beamforming, the number of antenna paths can become so large that transceiver and front-end chips are duplicated. In this way, a transceiver becomes a complex compound of multiple chips that is augmented with an antenna array. As a result, the packaging level will require advanced PCB technology or heterogeneous 2.5D / 3D integration. In such technologies the interconnect pitches must be small, and losses need to be low, both in the interconnect and in the transitions to the chips (e.g., via micro bumps). Low losses are again beneficial to minimize energy consumption.

As several European companies and research groups (among which the large RTOs imec, CEA-Leti and Fraunhofer) are strong in this domain, a transfer of this know-how to the industry is an opportunity for Europe to play a stronger and critical role at a higher level in the supply chain than solely at the level of chip design and processing.

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3.2.1.1.1.9. Efficient testing of analog, RF and mm-wave circuits

Time and cost of design including testing is still limiting the development of Analog/Mixed signal ICs even for SoCs with a dominant digital content. Improvements are still required for Analog/Mixed signal design productivity and predictability.

Entering the mm-wave frequency makes transceiver testing even more challenging. An important reason is the higher sensitivity to electrical parasitic as already mentioned above. The other reason is the use of beamforming. Measuring the beamforming functionality with wafer probes is not practical. Instead, the compound of one or more chips and the antenna array can be characterized with tests over the air. This can lead to time-consuming measurements with complex setups where calibration is difficult. Know-how in the field of characterization of mm-wave communication systems is important to foster in Europe to help the mm-wave IC design companies.

3.2.1.1.2. Mid-term needs

3.2.1.1.2.1. GaN at mm-wave frequencies

Just as for the microwave frequency region, RF GaN is considered as a technology to generate higher transmit powers beyond the capabilities of silicon technologies. However, this requires downscaling of the channel length of GaN HEMTs to achieve the speeds required for mm-wave operation, while reliability still needs to be maintained. Worth mentioning is the availability of GaN PAs for defense applications (K-band) which is a critical support for development of a new generation of GaN PAs for E- and D-bands. Further, the nonlinear behavior of GaN HEMTs, that has already been mentioned above, might again call for predistortion, which is more challenging than in the microwave region as the symbol rate at mm-wave frequencies is higher.

3.2.1.1.2.2. Design of D-band transceivers

To cope with the insatiable demand for more data, backhaul is challenged to accommodate ever increasing data rates. The adoption of wireless backhaul avoids drastic infrastructure works that are typically needed to install wired backhaul. The high data rates can be obtained by using the bandwidths that are available in the D-band. The combination of wider channels and spectrum efficient methods can be used for ultra-high-capacity backhauling and Fixed Wireless Access (FWA).

In the D-band, beamforming will be used with even more antennas than at mm-wave frequencies. This will be needed to compensate the limited power gain of the active devices at these frequencies and the large interconnect and distribution losses. The active circuitry needs to be connected to a large antenna array. To avoid grating lobes in the antenna pattern of the phased array, the pitch of the antenna array patches should not be higher than half of the wavelength λ in free space. At 140 GHz, λ/2 is 1.1 mm. To avoid a messy routing between the ICs and the antenna array, this pitch should be adopted for the ICs, which is quite challenging. The result is that beamforming transceiver design comes down to co-design of IC, package and antenna. Extra complications are high losses in on-chip interconnect and in the chip transitions, potential interactions between the chip and the chip carrier.

It is expected that as much transceiver functionality as possible will be implemented in one of the fastest CMOS technologies such as 28nm planar bulk or 22nm FDSOI while for the rest of the functionality, especially for the generation of transmit power, technologies like SiGe BiCMOS

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and InP will be used, as will be discussed in the next section. The use of multiple IC technologies is again an extra complication.

From the above reasonings it is seen that D-band transceiver design is challenging, requiring skills in mm-wave IC design, classical microwave theory of distributed elements, packaging, and antenna design. If Europe wants to address these challenges, then it should timely invest in training students and young engineers in those skills. Moreover, a European vision is needed on how to keep sufficient engineers in such IC design activities.

Another complication is the testing of these transceivers. This problem has already been described in Section 3.2.1.1.1.9 for mm-wave transceivers but at sub-THz frequencies these challenges are even more pronounced.

However, several silicon technologies, including CMOS ones with an f_{MAX} just below 400 GHz, can be used to design most transceiver functions except for the power amplifier (PA). For the latter, HBTs can be used from SiGe-BiCMOS or, for even higher powers, high-mobility materials such as InP that combine a high f_{MAX} with a supply voltage well above 1 Volt. For the highest energy efficiency, InP is the best choice for generation of transmit power at sub-THz frequencies.

D-band transceivers should also consider the interface to the baseband section through the data-converters (analog-to-digital, digital-to-analog). Although large bands up to 20 GHz will be processed by the RF front-ends at D-band, the delivery of these signals to the base-band unit will be very challenging as the data-rates approach several tens of Gb/s. The power consumption of the data converters becomes very important for sampling frequencies beyond a few GS/s. Therefore, the overall baseband-to-RF interface and the RF transceiver frequency plan have to be optimized jointly to find the optimal tradeoff at each stage of signal processing. Parallelization (or channel bonding) may offer a solution to the data-transfer bottleneck by relaxing the required sampling rate on the digital to analog interfaces, but this imposes some constraints to the overall radio architecture and base-band signal processing because the number of simultaneous channels is increased. Mastering these issues requires a good understanding and training on both analog and digital signal processing and represents an opportunity for European education and research institutions.

The partitioning of the transceiver architecture is also another challenge to be solved. The (high-speed) baseband processor will not necessarily be implemented in the same technology than the RF transceiver and the data converters should be included in one or the other chip. The interface between the two units (RF and baseband) then becomes critical, involving advanced packaging and high-speed digital signal or wideband analog signal routing depending on where the data converter stage is integrated, an issue that is common to wireline links.

3.2.1.1.2.3. Non-CMOS integration technologies for D-band transceivers

The speed limitation of CMOS necessitates the use of other technologies. Especially for an efficient generation of power, SiGe BiCMOS and InP are superior over CMOS. The aspect of energy efficiency is very important as wireless communication in the sub-THz frequency region will require much more base stations than for lower frequencies as the propagation losses between base station and end users increase with frequency.

For the implementation of the active circuits in the highest-frequency part of a transceiver, the fMAX of the device should be a factor five higher than the operating frequency. This is challenging for the SiGe-BiCMOS technologies that have been published so far. The fastest SiGe

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HBT published so far is from IHP and it has an fT/fmax of 505 GHz/720 GHz. Further developments are needed to increase the speed of next-generation SiGe BiCMOS generations such that enough design margin is obtained.

Indium Phosphide (InP) devices, on the other hand, already attain speeds that provide this margin, both for HBTs and for HEMTs. Europe has several foundries and research centers with know-how in fabrication of high-mobility III-V devices. However, these technologies today are still niche technologies and very expensive, making use of small wafers (e.g., 100 mm). Here is a great opportunity for Europe to deploy InP to a level that can serve a mass market: elements to consider are the use of larger wafer sizes and Cu metallization, improvement of yield, reliability, compact modelling, foundry services with available PDK, ... Just as with GaN, where silicon wafers are already used as a low-cost alternative to SiC wafers, one could also consider 200 mm or 300 mm silicon wafers as a starting material and grow or reconstitute the III-V material onto silicon instead of starting from a native, smaller InP wafer.

Next to the IC technologies, there will be a need for a 2.5D or 3D packaging technology that allows for the complex combination of multiple chips with an antenna array, while featuring low interconnect losses, with sufficient possibilities for heat spreading and heat evacuation, ... This also comes with the requirement of finer pitches and a high reproducibility for the interconnects.

3.2.1.1.3. Long-term needs

3.2.1.1.3.1. Wireless transceivers for IEEE 802.15.3d

On a long term, the G-band will be used for wireless communication at extremely high data rates, theoretically up to 315 Gbps in the IEEE 802.15.3d standard [Pet20]. Research has already published silicon-based transceivers for this frequency band, but these are based on harmonic generation as the operating frequency is very close to or even above f_{MAX}. This leads to very low efficiencies. A more efficient and robust approach would be to rely on fundamental frequency operation of the transistors instead of at harmonics. This is only possible if f_{MAX} is sufficiently high above the carrier frequency, which could be accomplished with InP [Urt16] and future SiGe HBT technology. Further, co-design of the chips and package that includes the antenna array will be even more critical than in the D-band. Here again, Europe should bank on know-how that is being developed in European research on packaging and heterogeneous integration (see e.g. [Hei21]).

3.2.1.1.3.2. New materials for active devices

Instead of pushing the speed of the classical device architectures in silicon or compound semiconductors, research on the use of so-called 2D materials (graphene, hexagonal boron nitride (h-BN), transition metal dichalcogenides (TMDs), silicede, and phosphorene) for new device types is already ongoing today. Some of these devices are promising to extend electronics to frequencies where performance of classical devices is degrading: resonant tunneling diodes, which can find applications as oscillators operating at several hundreds of GHz, nanowires, ...

This research requires the combination of materials research, device physics and fabrication aspects. While such know-how is present in Europe, research for new devices should be timely steered to industrially relevant applications.

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3.2.1.1.3.3. Wireless transceivers using microwave photonics

The advance of integrated photonics technologies (silicon photonics, III-V-based photonic ICs) have been adopted in optical networks in telecom infrastructure and datacenters. So far, wireless transceivers consist of circuits that are purely based on electronics, not on optics. However, the unstoppable hunger for higher wireless data rates will drive the search for new spectrum to ever increasing frequencies where optical approaches might become superior for some functions that today are made with electronic circuits.

With the availability of quite some photonics platforms, both silicon-based and III-V based, EU is well positioned to explore the usage of photonics for some functions in transceivers such as sub-THz frequency generation with a high spectral purity, filtering and beamsteering functions.

3.2.1.1.4. European strategic position and potential - SWOT

This section contains a translation of the descriptions above into a SWOT analysis. For clarity, we show different tables, starting with a general one and then specific ones on design and technologies, for which a separate analysis is appropriate.

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3.2.1.1.4.1. General SWOT analysis for wireless infrastructure

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• Good foothold in major telecom system manufacturer market player, who are manly European, as NOKIA, ERICSSON and SIAE. • Strong system knowledge, either got by internal R&D or biz partnerships. • Strong analog design competences. • Presence of leading suppliers of mature and derived IC technologies • Dynamic small and medium enterprises • EU has much know-how - both at industrial level and in research - on packaging, 2.5D/3D integration • EU is preparing for 6G via several initiatives (5G PPP, flagship, Horizon Europe, NetworldEurope, ...)	• Few examples of technological ecosystems; Ecosystems related to microelectronics are drying up in EU • Heavy reliance on imported semiconductors for electronics and optics • Few standard products to play active development role • ASSP requires high investment in application support • RF & mm-Wave IC design know-how increasing, yet to be improved. • High investment requirements to create or maintain competitive technology advantage • Missing main IPs both Digital and Analog
Opportunities	*Threats*
• Explosive growth of wireless market expected • Getting worldwide market leadership in 5G and beyond network wireless backhauling and the just increasing FWA market • Increment of incentives from EU governments to establish new fabrication plants • Foreign investments to expand the growing facilities all around Europe. • Increasing mobile data consumption is driving new network architectures and frequencies • Innovative solutions required for lower energy consumption in combination with high performance •	• Photonic and Electronic chip shortage • Strong dependencies in supply chains • Lack of ability to make own strategic decisions due to strong dependencies (e.g. on chips in advanced CMOS designed/fabricated outside EU) • Market evolution uncertainty due to COVID, climate change, and geopolitical tensions • Other regions are organizing themselves to prepare for 6G • Non-EU competitors have very aggressive product portfolio and expertise, making high barriers to entry • Undefined standardization and uncertainty on future requirements on 5G and beyond network can determine loss of R&D investment. • Network operators may have potential cash problem to improve the network, reducing the volume, thus ROI • Rapidly growing Chinese suppliers

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3.2.1.1.4.2. SWOT analysis for IC (digital, analog, RF) and packaging design

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths

- EU has several strong digital, analog and RF IC design teams (large companies, SMEs, research)
- Education level in EU universities/research centers is high
- Strong focus and good progress on heterogeneous integration at research institutes (CEA-Leti, Fraunhofer, imec, …)
- EU is well positioned in research for photonics design

Weaknesses

- Large fabless IC design companies are outside EU.
- Ecosystems around IC design in EU are drying up
- Every year less papers from Europe at flagship conferences ISSCC and IEDM
- For sub-20nm logic technologies EU is following a fabless approach as far as design capabilities are available (today)
- Less engineer students with analog/digital/RF IC design knowledge are graduating

Opportunities

- Adopting new frequency bands (mm-wave, sub-THz) and beamforming will need development of new transceiver architectures
- Building-up digital IC design capabilities in sub-20nm CMOS technologies as first step towards leading edge manufacturing in Europe in the long run
- Product development and even prototype development of 6G transceivers did not start yet at industrial level. Now is the time to start.
- Focus on RF integration delivering breakthroughs in size, weight, and cost
- Use SiGe-BiCMOS for sub-THz design
- Design of heterogeneous integration for sub-THz
- Focus on the design of RF-frontend modules (heterogeneous integration): Complexity of RF-frontends continues to grow fast

Threats

- For chip fabrication in advanced CMOS, EU depends very much on Asian manufacturers mainly from South Korea and Taiwan (today)
- Strong dependence on US suppliers of design tools
- Lack of security in chips due to strong dependencies from other regions
- IC design flow complex and design productivity low for mm-wave and sub-THz frequencies, requiring co-design of chips, antenna array and packaging.
- EU might fail to attract sufficient IC design talent (too few students, unattractive salaries, small ecosystems)
- Testing of ICs for mm-wave and sub-THz is time consuming and expensive
- Asia's R&D moving at accelerating speeds and North America's leadership in leveraging academic innovation and shortening the path to productization can easily outperform Europe's race for mm-wave and sub-THz championing in 6G.
- Rapidly growing Chinese R&D community

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3.2.1.1.4.3. SWOT analysis for logic, RF IC and packaging technologies

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• EU has strong research on very advanced logic and RF device technologies and advanced 2.5D/3D integration • Strong R&D in photonics technologies • Strong focus and good progress on technologies for heterogeneous integration at research institutes (CEA-Leti, Fraunhofer,imec, …) • Good position in devices for power management (Power-GaN, SiC, …) • Strong EU position and roadmap in BiCMOS and SiGe-HBT technology • EU strong in SOI, RF-SOI, FD-SOI, ….	• Manufacturing of latest logic CMOS technologies not available in EU today • So far, no large commercial European fabrication chain for InP (industrial III-V activities focused on GaAs and GaN) • Ecosystem for InP not well developed • Spillover from research to device and packaging technologies is limited • EU Not competitive in RF-GaN for commercial applications (RF-GaN market for commercial applications it completely dominated by US and Far-East) • Little focus on very relevant technologies like research on vertical GaN devices and new substrates like diamond • Heterogeneous integration and advanced packaging are key enabling technologies for future connectivity circuits and systems, but Europe lacks strong ecosystems in this area.
Opportunities	*Threats*
• Building-up chip design capabilities for latest chip technologies as first step towards leading edge manufacturing in Europe in the long run (< 2026) • Attracting investments by non-European chip manufacturers in Europe or joint ventures with European chip manufacturers for latest chip technologies as first step towards European manufacturing (<2026) • Building up European manufacturing sites for latest logic technologies (> 2030) • RF GaN-on-Si more environmentally friendly and cheaper than GaAs • Usage of mm-wave and sub-THz band triggers development of packaging technologies and device technologies (BiCMOS, InP) that overcome speed and power limitations of CMOS • Deployment of RF GaN and InP helped by existing know-how in EU on GaAs	• For leading edge technologies EU heavily depends on manufacturers from South Korea and Taiwan • Strong dependencies in supply chains • Lack of ability to make own decisions due to strong dependencies (today) • Global competition in III-V technologies: Industrial background in the US already available (also due to DARPA and other defense funding) • Mm-wave/sub-THz: investments to increase speed of devices are expensive • Nonlinear effects in GaN can complicate its usage for very high data rates at which digital predistortion is too power-consuming • Rapidly growing Chinese foundries (and suppliers)

3.2.1.1.5. Identified key strategic actions

The list of actions below follows from all considerations in section 3.2.1.1.

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Short term (<2026)
• Deploy 5G in EU as thoroughly as possible • Increase resources on digital IC in leading edge logic technologies • Building up mm-wave transceiver and front-end design capabilities • Educating people in new skills on chip design (advanced digital, mm-wave and sub-THz) and manufacturing technologies • Attract investments from non-European chip manufacturers in Europe or joint ventures with European chip manufacturers for latest logic technologies as first step towards European manufacturing based on advanced logic technologies. • Launch EU funded collaborative RIA projects on telecom applications operating in the W-band (75-110 GHz) and D-band • Define 5G/6G system requirements for semiconductor components and participate in 5G/6G standardization. • Build demo systems based on OpenRAN, campus networks, and vehicle-to-X communications; • Invest in high-frequency, thermally efficient packaging substrate technologies with embedded antenna array elements. • Research on integrating InP and GaN devices on silicon • Research on efficient testing of mm-wave and sub-THz circuits • Create incentives that stimulate startups in microelectronics design • Create incentives to attract students to microelectronics design (analog/digital/RF) • Continuous investing in technology R&D, focusing on developing <28nm FDSOI and SiGe HBT with f_T, f_{MAX} > 600GHz
Medium term (2026-2030)
• Building up manufacturing facilities in Europe in form of joint ventures or by investment on non-European vendors • Launch EU funded collaborative RIA projects on telecom applications operating in the W-band (75-110 GHz) and D-band • Continuous investing in heterogeneous integration technology R&D • Grow ecosystem around InP, including co-integration with silicon • Grow RF-GaN capacity • Develop industrial prototypes of 6G communication systems
Long term (>2030)
• Building up European manufacturing sites for sub-10nm technologies • Optoelectronic based mm-wave and sub-THz generation and processing by heterogeneous integration with photonics technologies (silicon photonics and III-V-based). • Deploy 6G in EU as thoroughly as possible

3.2.1.2. Wired infrastructure

The quest for more data is not saturating in the foreseeable future. This will result in a growth of the infrastructure shown in Figure 16, of the number of the data centers and of the baud rate in the wired networks. Copper cables in the access networks will be gradually replaced by fibers (FTTH). Today, commercially available optical transceivers used inside datacenters obtain speeds around 56-75 Gbaud per lane, but next generations will require 120...180 Gbaud and even more. Roadmapping in this domain must consider that the market of datacenters and infrastructure networks is smaller than the automotive market and certainly significantly smaller compared to the mobile handset market. The datacenter market is largely dominated by webscale companies (e.g., Facebook, Amazon, Microsoft, Google, and Apple) that even implement their own equipment. Inside data centers, traffic is routed via a hierarchically arranged network, consisting of (top-of-rack) switches and (optical) high-speed links. The short-term challenge will be in increasing data traffic handled by such switches to 51.2 Tb/s, with

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100Tb/s already on some industrial roadmaps. Scaling the capacity of such switches to the 100Tb/s range will require drastically limiting power consumption, for which Co-Packaged Optics (CPO), a technology that co-integrates optics and ASICs, is a strong contender. Microsoft and Facebook have launched the CPO initiative in 2019 to enable the development of common design elements that will guide technology vendors (like Broadcom). Similarly, NVidia is working on versions of its NVLink and NVSwitch relying on co-packaged optics to reduce the power consumption in the IO's of their switch and network ASICs. Electrical and photonic IC design and manufacturing activities in Europe for this market have been reduced over the years, one of the reasons being the limited market size. However, Europe still holds several low-volume open platforms both in industrial and research labs (imec, CEA-Leti, IHP, FhG, LIGENTEC, VTT, Smart photonics, HHI, Jeppix). Moreover, next to optical communication, photonics is present in many other domains. A large growth in these domains could boost the growth of the photonics industry, from which the optical communication market could benefit. An example of such potential 'trigger application' is the photonics-based glucose sensor in the Apple Watch or the Lidar technology for the autonomous cars.

3.2.1.2.1. Short term

Scaling of optical transceivers to higher baud rates comes with extra complexity. Optical transceivers consist of four main sub-components: the modulator and demodulator/detector optics, the analog driver & receiver electronics (e.g. fabricated using RF CMOS or SiGe BiCMOS processes), the laser and finally (in many cases) a complex (DSP) SoC integrated using scaled CMOS. Product prototypes of such SoC's using sub-10 nm CMOS have been demonstrated by several companies, many outside Europe. Few counterexamples exist such as Nokia who is designing its own 7nm DSP for 90GBaud/400G and 600G coherent systems. From there we see a trend towards more digitization, requiring very high-speed data converters with a medium-high resolution (5-6 effective number of bits) and advanced packaging techniques such as MCM (Multi-chip Modules) to avoid loss at frequencies ≥ 100GHz. It shows to be challenging for European companies to increase their market share; creating design IP in such scaled technologies implies to compete with large established players in the field.

3.2.1.2.2. Mid-term

On the mid-term, the saturation of the speed of CMOS devices, as discussed in the introduction of Section 3.2, can become a showstopper to further increase of the baud rate per lane in future transceivers for applications beyond 1Tb/s (>200 Gbaud). Here is an opportunity for non-CMOS technologies that feature devices that are faster than CMOS ones, such as BiCMOS and InP.

As already mentioned in Section 3.2.1.1, the speed of the HBT in SiGe BiCMOS technology should be increased to leave sufficient design margin that is needed for robust design. Further, InP technology should be upscaled to a higher level of maturity (cost, throughput, yield). In this context it is also very relevant to consider efficient heterogeneous integration and chiplets. Worth mentioning is the new architecture design of very high-speed data converters (>100 GS/s) conducted by leading research teams in Europe (imec, University of Stuttgart, University of Saarland, III-V Lab, etc.) on analog multiplexing and demultiplexing that could offer new opportunities to further extend transceiver speed.

At a higher level in the supply chain, the packaging of transceiver modules will become more complex as the increase of the data throughput not only comes from an increase of the baud

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rate per lane but also in an increase of the number of wavelengths, requiring more lasers. Photonics packaging is an activity already present in European research centers (Tyndall, imec, FMD, ...) and a transfer of this know-how to industry could be a means to cultivate European players in this domain.

3.2.1.2.3. Long term

The challenge to solve for the longer term is how to achieve far beyond 100 Gbaud operation in a cost-effective, densely integrated and energy-efficient way with the constraint of speed limitations and/or high losses of current electronics and optics. What are cost-effective and industrially scalable material systems offering O/E (optical-to-electronics) and E/O (electronics-to-optical) bandwidths well above 100 GHz, while simultaneously offering monolithic integration of passive components such as wavelength MUX/DeMUX, polarization handling, fiber coupling? What is a cost-effective and industrially scalable method to integrate the laser? InP might be a suitable material here, again implying the need for upscaling InP technology, not only for transistors, as mentioned in Section 3.2.2.3.1, but also for optical components like lasers. Further, new materials could be investigated to address these questions. Other options for ultra-high-speed opto-electronic modulation could be the use of materials such as BTO or LiNbO3 on Silicon as a cost-effective means to realize high-speed opto-electronics or plasmonic modulators. Especially BTO is an interesting option as it allows for integration of modulators with small footprints inside a CMOS fabrication line (unlike even thin-film LiNbO3).

For backplane transceivers the transmission of radiowaves over plastic fiber could be an interesting solution for the future. Initial research in this area with very strong European involvement shows very convincing results demonstrated in lab demos. With this technology data rates of up to 100 Gbps over several meters at comparably low power consumption can be achieved. Further it is evident that by increased bandwidth at higher frequencies (beyond 200 GHz) and dual polarization, the data rate and link distance can be significantly improved.

So far, only digital optical transceivers have been addressed, in which symbols or bits are transported over fiber. With higher RF carrier frequencies being considered for wireless systems, the cell sizes in cellular networks are ever decreasing, while simultaneously the amount of traffic that needs to be transported to and from the baseband antenna masts are ever growing. This effectively implies that optical fiber is ever getting closer to the antennas themselves. Use of advanced radio techniques such as beamforming, MIMO etc. is set to further accelerate the amount of data that needs to be moved to and from the antennas and base stations. Alternative approaches to move this fronthaul data may then become increasingly important: for example one can envision technologies such as analog radio-over-fiber or hybrid forms being used to deliver RF signals to and from antennas. Additionally for some functionality such as beamforming optical techniques may have advantages compared to purely electronic techniques. Such microwave photonics could start to play a role at ever higher carrier frequencies, especially if integration and assembly costs of opto-electronics go down.

3.2.1.2.4. European strategic position and potential - SWOT

Based on the considerations above, the following SWOT table can be constructed.

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Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• EU has strong research on photonics technologies and optical transceivers • Several EU platforms for photonic ICs • EU is strong in advanced packaging • Strong in RF IC technologies (BiCMOS, FDSOI) • EU dominates research on radio waves over plastic-fibre (PMF technology)	• EU does not have a strong industrial player anymore in datacenter and optical communication chips • Not enough focus and involvement in silicon photonics research in Europe • EU lags behind in design (and fabrication) of scaled CMOS IC, which are one of the critical parts of optical transceivers operating at very high baud rates
Opportunities	*Threats*
• Higher data rates and strong growth of number of end users (human + machine) requires strong growth of base stations and access points shorter to end users • Roadmap of optical transceivers with data rates doubling every 2-4 years continues for at least another 2-3 generations • Access via copper wires will need to be replaced by fiber access or FWA • More digitization in optical transceivers with ever increasing speed requires design of fast ADCs/DACs and complex digital transceiver ICs including DSP • Saturating speed of CMOS gives opportunities to involve EU BiCMOS technologies in optical transceivers • InP can cope with the increase of speed of optical transceivers beyond the capabilities of any silicon technology • Adoption of photonics components in industries outside telecom might boost the EU ecosystem of photonics platforms • Co-integration of optical transceivers and switch ASIC and trend to laser miniaturization requires heterogeneous integration of chips with photonics components • The new PAM4 interfaces (instead of LVDS) are supporting PMF (Plastic Microwave Fiber) technology	• Big players outside of EU grow fast and move on quickly to the design of ever higher-speed optical transceivers and transceiver modules • Many EU SMEs involved in photonics integrated circuits chip design acquired by non-EU companies

3.2.1.2.5. Identified key strategic actions

Short term (<2026)

- Establish components (photonic and electronics) that facilitate optical transceivers with baud rates 100…130Gbaud: modulators and detectors with bandwidths of at least 80GHz; front-end driver and receiver electronics with analog bandwidths between 60GHz to 90GHz; analog-to-digital and digital-to-analog convertors integrated using scaled CMOS with sampling rates >>100GS/s, analog bandwidths >50GHz and 5-6bit ENOB.
- Establish components (photonics and electronics) with a very strong focus on ultra-high channel counts (100s of channels), integration density (>>100Gb/s/mm), and energy efficiency (< 1pJ/bit) to facilitate co-packaged optical interfaces on new generations of switch ASICs, GPU's, CPU's.

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Medium term (2026-2030)
• It is required that the datarate for all the various IO standard doubles every four years to avoid limiting the performance scaling of the systems. In the medium term this implies a focus on beyond 180Gbaud operation. For co-packaged optics, further scaling in terms of integration density, larger channel counts, low energy requirements will be crucial. • In part this improvement is enabled by process scaling but it also requires significant advances in energy efficiency, equalization,clocking and reliability • In Europe significant investments in RIA programs will be needed to be part of this development • Focus on new process technologies for photonics that allow E/O and O/E conversion bandwidths beyond 100GHz • Deploy IC technologies (SiGe BiCMOS, InP) that allow integration of functionality with bandwidths far beyond 100GHz • Integration approaches for photonics and electronics that allow a dense integration of a large amount of connections with bandwidths in excess of 100GHz (MCM, 3D)
Long term (>2030)
• It is required that the datarate for all the various IO standard doubles every four years to avoid limiting the performance scaling of the system. Could we envision system baud rates far beyond 200Gbaud? • Research into novel optical transceiver architectures, where functionality is shifted further into the optical domain: optical-domain equalization, optical-domain interleaving

3.2.2. Consumer grade connectivity

User equipment (UE) is by far the largest market for wireless communication devices. In the market that we know today (cell phones, tablets, laptops, smart watches, ...) there is no big European player anymore. Europe has lost this market both at the level of end products and at the level of complex digital chips and transceivers.

Regarding transceiver chips in the microwave region, these have almost become a commodity for sub-6 GHz 4G LTE and are designed in advanced sub-20 nm CMOS generations by Far East and USA companies. For 5G user equipment a similar scenario is about to happen – both for FR1 (410 MHz – 7.125 GHz) and FR2 (24.25 GHz – 52.6 GHz) – by lack of a big European player. Hence, intruding into the transceiver IC market for 5G and beyond looks very difficult on the short term. In the communication part of UE there are only EU players left in the front-end electronics between the transceiver chips and the antennas.

UE will evolve from devices operated by humans to a mix of human-centric and machine-centric devices, giving rise to an explosion in the absolute number of devices. For technologies such as virtual and augmented reality tremendous data rates are needed, which will necessitate the adoption of the FR4 spectrum (52.6 GHz to 71 GHz) and above, including sub-THz spectrum. UE will communicate with an access point or base station (can be an indoor one) which will have to follow the same data rate increase. An explosion of the number of end users is only sustainable if there is a strong reduction of the energy consumption per useful bit of data, even more than for infrastructure. Further, the pressure on cost and form factor is much stronger for UE. Next, the required transmit power for the uplink is much smaller than for a base station due to lower uplink data rates compared to the aggregated downlink data rate. These boundary conditions have several consequences. First, given the large market size, economics of scale will drive the big IC design players to transceiver design in recent CMOS nodes, combining the analog/RF transceiver functionality with the complex digital modem. For microwave frequencies, where beamforming is not applied, silicon-based transceivers are aided by III-V-based power amplifiers. Today, GaAs is widely used. For the lower mm-wave frequencies (28 GHz, 39 GHz)

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beamforming with a limited number of antennas (< 10) is used in UE. Thanks to this beamforming, the required transmit power per PA is limited and it is in reach of CMOS, although the EIRP can still be higher with heavy-duty III-V-based PAs. The first wave of 5G cell phones that are available at this time of writing are CMOS-based, extension with non-CMOS PAs might be foreseen for next generations if price permits.

3.2.2.1. Short-term needs: front-end modules

Front-end modules for UE constitute the only space where Europe can still play a significant role on the consumer connectivity market leveraging the derivative technologies developed by major European IDMs. Just as for wireless infrastructure (see Section 3.2.1.1.1.3), front-end and RF filter design at microwave frequencies is a domain in which European industry should remain active in order not to completely lose the wireless consumer market on the short term. The filtering problem at mm-wave frequencies is less severe than at microwave frequencies due to the spatial filtering by the beamforming and the higher path loss at mm-wave frequencies. For the higher mm-wave frequencies and the D-band, beamforming is also used, but the limited power gain of silicon-based devices might necessitate the use of III-V-based power amplifiers, which results in a mix of several chips in several IC technologies, leading to a higher complexity of the front-end modules. The performance gain from the use of multiple IC technologies should be traded off with the cost of the front-end module.

3.2.2.2. Mid-term needs

3.2.2.2.1. mm-wave transceiver IC and module design

While the wireless consumer market for sub-10GHz transceiver chips is consolidated, without the presence of large EU players, there is still an opportunity at the mm-wave frequency bands. For frequencies above the FR2 band of 5G and for the sub-THz band, the number of antennas that will be used for beamforming will be so large that the transceiver functionality will be divided over multiple chips such that the drive for single-chip modems is heavily attenuated. Instead, an assembly containing multiple chips and antennas is a realistic scenario. Also, here EU industry could capitalize on the know-how on heterogeneous 2.5D/3D integration and advanced packaging technology research in Europe integrating chiplets of transceivers, digital basebands (all manufactured outside the EU) in a heterogeneous fashion with front-end active and passive components and antenna arrays. Further, when due to the splitting of the beamforming transceiver functionality over multiple chips in case of large antenna arrays, the analog/RF transceiver functionality no longer resides on the same chip as the digital modem, cheaper and faster Si technologies than recent CMOS node technologies can be considered such as BiCMOS and FD-SOI. Several of these technologies from European foundries could be used here, provided that the fabrication capacity is large enough. While this capacity is not sufficient today, EU BiCMOS and FDSOI foundries should reflect on this.

Finally, the market of mm-wave transceivers operating above FR2 frequencies is still small and European players could consider stepping into this market.

3.2.2.2.2. RF GaN-on-Si to replace GaAs

Today, the cellular mode in mobile phones requires Watt-level output powers that are difficult to generate with CMOS. Instead, the power amplifier technology that is used nowadays is GaAs pHEMT. RF GaN on silicon, as already mentioned in Section 3.2.1.1.1.6, is a cheaper alternative

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of GaN on SiC. It is expected that the output power and the efficiency of GaN-on-Si HEMTs is comparable to GaAs, while it is less toxic than the latter material. The low cost and the lower toxicity can make GaN-on-Si a serious contender to replace GaAs in handsets.

3.2.2.3. Long-term needs

3.2.2.3.1. Module design for D-band communication

The adoption of the D-band in user equipment will probably come later than in infrastructure, where wireless backhaul is expected to use the D-band already on the mid-long term. Augmented and virtual reality will ask for wireless data rates of at least several tens of Gbit per second, requiring large RF bandwidths, which can be made available in the spectrum above 100 GHz. Just as for the mm-wave frequencies below 100 GHz, the transceiver functionality will be split over multiple chips as beamforming will be used. If for the D-band the same footprint for an antenna array in user equipment is used as today for 5G at 28 GHz, then the array for the D-band, the middle of which is 5 times higher than 28 GHz, contains 25 times more antennas. Further, due to the limited power gain and the limited power supply voltage of CMOS, transceiver design for the D-band will be extremely challenging. It is now time to prepare such transceiver design in Europe, as Europe has analog IC design skills but also some technologies in production and in research that will be needed to complement CMOS due to its limited speed and power capabilities. These technologies are discussed in the next section.

3.2.2.3.2. Non-CMOS technologies for D-band

As already pointed out in Section 3.2.1.1.2.3, InP is the best implementation technology for the power amplifiers as it yields considerably higher output powers and efficiencies in the D-band. Here then come some opportunities for Europe:

- InP technology should be brought to a level where circuits like PAs can be fabricated in a cost-effective way, such that the 6G UE market can be served.
- Heterogeneous integration, combining InP with silicon-based technologies as well as antennas and heatsinks in a cost-effective way (including high reliability) is an activity that can back on several research in Europe about InP technology and heterogeneous integration.
- Europe should make sure that sufficient design engineers are trained for this very specific design of the analog/RF transceiver functions using InP.

BiCMOS could still play a role here as well: although SiGe-based power amplifiers will have a lower efficiency than InP-based ones, the advantage of the SiGe that it is a much more established technology, with a much more developed ecosystem and cheaper than InP today. However, the expected volumes of 6G user equipment go well beyond today's SiGe fabrication capacity. Committing to BiCMOS here requires a significant increase of BiCMOS processing capacity.

3.2.2.3.3. Joint communication and sensing

Applications like Augmented Reality require both sensing and extremely high-data rate wireless communication. The sensing and the communication will need to be well synchronized and a low latency will be crucial. In addition, the large signal bandwidth that will be foreseen for communication in the mm-wave and sub-THz frequency regions, in combination with the high

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operating frequency, is favorable for a good resolution of range, speed and orientation in sensing with radar. Research is needed on how to realize hardware and signal processing software that can combine radar and communication with no penalty on performance while being more economical and compact than just putting the two technologies next to each other.

3.2.2.3.4. Low data rate wireless UE devices

With the advent of 6G, a new, potentially large market might appear for devices that wirelessly connect a huge number of various appliances (whitegoods, gardening and household tools, different kinds of sensors, cameras, ingestibles, skin patches, wearables, ...) to user equipment or to small base stations. In many cases, the data rate for information exchange is very low. Also, complexity of the edge computing in many of these devices might be relatively low, such that there is no need to use recent node CMOS. This market, which might become an important one, will not be challenging for the IC technologies. The challenge will be more on the power consumption and the form factor of the module. Hence this is an opportunity that Europe could decide to take with low-power transceiver design and advanced module and packaging development.

3.2.2.4. European strategic position and potential - SWOT

Several aspects that have been discussed in the SWOT analyses of wireless infrastructure also apply to consumer grade connectivity.

Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• EU contributes to parts of front-end modules in UE • EU has strong research in many technologies needed in 5G/6G equipment: logic and RF technologies, packaging, RF IC design	• There is no EU player anymore in UE end products • All big players in design of TRX ICs and digital modem and signal processing ICs are outside EU • TRX and digital ICs use advanced technology from outside EU • EU is losing design capabilities, both in digital with advanced technologies and in analog/RF • The ecosystem of InP, as the device technology that is superior for operation in the D-band, is very small in EU
• Carrier frequencies increase to mm-wave and sub-THz band, beyond speed and/or power capabilities of CMOS. This opens the door to the adoption in UE of IC technologies where EU is strong, either with established industrial players (e.g. BiCMOS) or research centers (III-V, III-V on silicon) • Adoption of phased-array technology in UE will create a large demand for complex 2.5D/3D integration	• A technology such as 6G will have a deep impact on our lives, the digital inequality will be an important point of attention • The broad deployment of 6G should remain sustainable in terms of energy consumption • Expected 6G volumes go beyond the worldwide installed capacity of non-CMOS technologies
Opportunities	*Threats*

3.2.2.5. Identified key strategic actions

In the field of consumer grade connectivity, it is probably an illusion to bring the design of complex chips in advanced CMOS back to Europe. Instead, it is best to focus on the strengths that are still present in Europe, namely the front-end circuits which do not use advanced CMOS. These modules will evolve to higher frequencies, will have to cope with the presence of antenna

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arrays due to the beamforming. With increasing frequency, the design of such modules will have to be done more and more in combination with the design of the active circuits.

Due to the economics of scale, transceivers will be implemented in CMOS as long as energy consumption and performance allow this. For the mm-wave frequencies above FR2, BiCMOS might be superior to CMOS as the fT/fMAX of SiGe HBT device can still be stretched while CMOS speed saturates. If BiCMOS gets adopted for UE operating in the 60 GHz band and above, then the capacity of BiCMOS today is probably too small and needs to be grown.

For circuits operating in the D-band, InP is intrinsically the best technology for power amplification and efficient power generation. But this will only be adopted if it can be deployed in an economical way at a sufficiently large scale. This will stimulate research on the integration of InP on silicon, and on larger (6") substrate size in InP.

Further, for the efficient generation of high transmit powers in the low-GHz and mm-wave frequency range, GaN-on-Si might be considered to replace GaAs as GaN-on-Si is more environment friendly and potentially less expensive than GaAs.

Short term (<2026)
• Maintain EU presence in UE front-end modules • Join forces of research and production on 2.5D/3D heterogeneous for UE equipment operating at mm-wave and sub-THz • EU should educate sufficient engineers to design complex modules based on 2.5D/3D integration combining digital, analog, mm-wave ICs and antenna arrays • Research for III-V-on-Si technologies that are economically viable for a large deployment: InP for sub-THz and GaN-on-Si as replacement of GaAs, larger wafer sizes for InP (6" and above). • For foundries of existing RF IC technologies: reflect on possibility to enter the market of transceivers operating above FR2 bands (requires capacity increase) • Continuous investing in technology R&D, focusing on developing <28nm FDSOI and SiGe HBT with f_T, f_{MAX} > 600GHz to prepare for front-end modules and possibly transceiver ICs according to previous item • Start research on joint communication and sensing
Medium term (2026-2030)
• Grow ecosystem around InP-on-Si for D-band applications • Grow RF GaN-on-Si capacity • Develop industrial prototypes for UE D-band modules combining heterogeneous integration and RF ICs some of which being developed in EU and processed with EU IC technology (Si and III-V)
Long term (>2030)
• Deploy modules on a mass-market scale for UE operating above FR2 band

3.2.3. Industrial grade connectivity

We focus here on key connectivity technologies (Low Power Wide Area, Bluetooth, WiFi, Ethernet, 5G) and microcontrollers required by industrial applications (basically industrial IoT, health and automotive). The strong European automotive ecosystem has provided a natural business opportunity for connectivity solutions developed in Europe. This comment can also be applied to other sectors, especially on the industrial market. However, another explanation also lies in the low cost and low power requirements of industrial applications which then call for the use of mature technologies. Most of the current MCU solutions are manufactured today in 90 nm CMOS with a slow transition to the 40 nm node (and below). Consequently, those markets are perfectly fitted for European IDM semiconductor manufacturers. This could also explain why Europe is having a key role on the MCU market.

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Industrial production is a major economic factor in Europe, accounting for around 25% of Europe's Gross Domestic Product. There is enormous innovation potential of IoT technologies when fully adopted not just in the production of physical goods, but in all activities performed by Manufacturing Industries, including pre-production (ideation, design, prototyping, 3D printing) and in the post-production (sales, training, maintenance, recycling) phases. Therefore, one of the major objectives of several European initiatives (e.g., Industry 4.0, Smart Factories) is to bring IoT paradigms to industry, production, and logistics [Ver15] demanding, amongst others, industrial grade connectivity.

From the end user perspective, i.e., production facilities taking up advanced connectivity solutions, this implies the availability of solutions that are tailored to meet demanding industrial requirements such as bounded latency and reliability, rather than more capacity. This not only implies the availability of chipsets, but the incorporation (or even customization) of such chipsets into industrial systems and their smooth and gradual integration into existing production environments (with a plethora of other standards and protocols), step-by-step and in a modular way. From a technology perspective, this opens opportunities to innovate across the entire value chain, from the smallest components needed to enable such connectivity up to the realization and integration of complete end-to-end solutions, possibly combining different communication systems. Further, the integration of communications and sensing may transform the way we perceive industrial grade connectivity. In this aspect, devices will sense, then locally process to some extent the sensed information and communicate.

Given the stronger starting position compared to consumer grade connectivity, industrial grade connectivity might be the best focus region for Europe to maintain and extend a position in microwave connectivity. Further innovations in design re-use by focusing on flexibility is of key importance (software defined MIMO transceivers). Moreover, combining flexibility with energy efficiency remains a key challenge and market opportunity. Maybe O-RAN developments and industrial connectivity opportunities can have interesting overlaps in mixed-signal processing and software defined transceiver hardware. Multi-market hardware may also be of interest to the European defense industry, where chip development is often not affordable given small production series.

Besides focusing on flexibility, one also needs to pay more attention to real-time operation aspects and realistic hardware/channel impairments. While much research is either focused on high-frequency (analog) technology research and digital PHY layer research based on theoretical concepts and simulations, many end-to-end system-level aspects remain unsolved.

Dedicated chip development (in particular digital signal processing) may become affordable in specific market segments when focusing on the right features. Standardized consumer-oriented chips (like cellular/WiFi) are too complex because of the requirements of backward compatibility. Such chips are closed and do not allow customization in smaller market segments. Backward compatibility is not a main requirement in many professional new markets and deployments, where chipsets with reduced but relevant feature set can perfectly do the job. Open chip design, with open driver and firmware are key to boost end-to-end innovation (from the PHY level to the application level).

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3.2.3.1. Short term

Europe has a clear leadership and can take advantage of a sizeable indigenous market thanks to strong industrial and automotive actors in Europe. Integration is also happening here, the capacity to design highly integrated solutions using more advanced nodes will have to be secured to maintain leadership. IoT will be a key driver for this market, but without any leadership on the cloud side Europe may capture a very limited part of the global value.

Compared to wireless transceivers for UE or RANs or transceivers in datacenters, transceivers operating in an industrial environment often need to function in harsh environments. Key requirements for industrial communication are reliability, bounded latency, robustness, etc. rather than capacity. 5G aims to target these requirements under the umbrella of URLCC, but the entire feature set (slicing, integration with Time-Sensitive Networking, etc.) will only come with R17, targeted for standardization in 2022 with devices 1-1.5 years later. This gives a window of opportunity of several years to focus more strongly on the design and realization of industry-graded 5G chips and complete end-to-end systems, including 5G-enabled industrial components that differ significantly from consumer devices. The more control over the lower-level building blocks and the less outsourcing outside Europe, the more room for innovation and end-to-end solutions that stand out.

Along with this, more uniformity in spectrum availability must be strived for to avoid fragmented markets. Further steps must be taken to step away from spectrum that is reserved at a large geographical scale and enabling spectrum allocations for local private industrial networks, as a stimulus for industrial competitiveness.

Further, as cellular technologies come with their own peculiarities (e.g., cost, complexity, etc.), the opportunities of the newly available unlicensed 6 GHz spectrum (or others for e.g. industrial use: e.g., 3.7 – 3.8 GHz in Germany for campus networks) must not be ignored. With its large bandwidth, interesting propagation properties and anticipated Wi-Fi 6E chips, its promotion should lead to parallel high-impact innovations for industrial connectivity that stand closer to current industrial communication systems, can also serve many indoor and short-range scenarios and a lower environmental footprint. To facilitate transitions in connectivity, technology interoperability must be given attention.

Accessible testbeds and trials are required to bring concepts to reality and validate whether solutions that have been driven by standardization in closed bodies dominated by limited big stakeholders can actually live up to the requirements of players within the industrial ecosystems, including the many SMEs in Europe.

3.2.3.2. Mid-term

On the mid-term, additional steps must be taken for Europe gaining more control over industrial connectivity solutions and systems. Within the context of 5G URLCC, openness in terms of O-RAN is simply not sufficient. Adopters of the technology are still bound to the interfaces provided by component providers, depend on the willingness of these providers to get more access or richer APIs, and are restricted with respect to end device innovations. Standardized open interfaces solutions can avoid such lock in situations compared to proprietary solutions.

To obtain trust in components and enable customization in a market that cannot have a one-size-fits all solution, approaches such as O-RAN must be further pushed down to the individual components, end devices and even chips. In January 2020, the possibility of the open-source

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movement entering and threatening the chip industry was discussed in [Kin20]. From economic reasons, economy of scale is necessary. This can only be achieved by standardized solutions and to ensure interoperability between components from different vendors.

Apart from potentially disrupting the chip industry, more open systems also have a role to play in educating students and could help to realize a better interplay between standardization and running code/HW. Due to the huge outsourcing efforts during the past decades, lots of expertise has left Europe and needs to be re-established to get back control on end-to-end solutions. Hence, efforts at the educational level must be foreseen to appropriately train engineering students, giving them more cross-disciplinary and applied hands-on training skills besides theoretical & high-level python design skills. By filling the gap between great analog design skills at one end and strong high-level software skills on the other hand, i.e., addressing real-time embedded and digital processing skills, engineers are formed that master the skills to understand complete systems.

In parallel to 5G's evolution in serving industrial communication, one should stimulate parallel innovations in communication, performed in collaboration with large industrial players within EU, and taking advantage of new unlicensed spectrum such as 6 GHz or local licensed spectrum. For instance, in [Pan17] the concept of Wireless High-Performance Communications was raised for building tailored industrial solutions, not built on general-purpose chips and having significantly lower architectural complexity.

Naturally, the quest to achieve ever higher data rates, but combined with industry-grade robustness, must be pursued for advanced, bandwidth-hungry industrial use cases. This requires components and solutions operating in the higher frequency bands (mm-wave and higher).

3.2.3.3. Long term

Sustainable radio communication infrastructure: reducing overall energy consumption per useful bit for data traffic (not only in end devices, but also in access, core and transport networks, (edge) clouds, also including energy consumption in control plane and traffic due to signaling and protocol overhead)

Push new radio architectures (like smart surfaces and cell-free massive MIMO) from the conceptual level to validated and affordable solutions beyond theoretical studies and simulations, considering hardware limitation and integration complexities (HW-SW integration, front-, back- and mid-hauling). This requires a lot of technology innovation across multiple disciplines, such as meta-materials, programmable intelligent surfaces and electromagnetics, on the one side and information theorists and signal processing experts on the other.

The higher-frequency bands with unfavorable propagation conditions may support the bandwidth-hungry applications. Still more efficient spectrum usage and spectrum reuse in lower frequency bands with excellent propagation properties can also be considered by using smart radio architectures. Cell-free massive MIMO, for example is capable to concentrate the wireless signals by minimizing interference and maximizing spectral reuse.

3.2.3.4. European strategic position and potential - SWOT

Based on the considerations above, a SWOT table can be made:

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Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths	*Weaknesses*
• Sizeable indigenous market with strong industrial and automotive actors • European leaders in industry-grade solutions, from large enterprises to dynamic small enterprises • Proven end-to-end wired-wireless system and domain knowledge to tailor connectivity solutions to industrial requirements • Industry 4.0 vision originated within EU and further being developed e.g. 5G-ACIA)	• Heavy reliance on imported general-purpose communication modules, lowering potential for low-level customizations and improvements • Loss of expertise on lower-level aspects (chip design, real-time operation, hardware acceleration…) due to outsourcing in the past • Focus of research and associated funding on higher-level software (architectures) and infrastructure, as EU depends on non-EU providers for chipsets and radio modems. • Global spectrum licenses limiting competitiveness • Lack of engineers with knowledge on complete end-to-end systems (from analog to high-level application software)
Opportunities	*Threats*
• Emerging market with full-blown (private) 5G URLCC only to appear in coming years • Newly available unlicensed 6G spectrum, opening opportunities for both cellular and WiFi technologies, the latter also evolving towards higher performance • Customization rather than mass production, well aligning with Europe's engineering and manufacturing powers • Increasing attention to openness (e.g. O-RAN, open chip design) to enable faster innovation • New radio architectures being explored as part of 6G research	• Dependence on non-EU providers of components and hence low-level access for customization • Standardization dominated by few big players, including non-EU competitors, introducing barriers to entry • Standardization to be driven by innovation, rather than blocking innovation (complexity, limited flexibility …) • Failure to attract and educate engineers within EU • Ignoring competing technology evolutions (e.g., WiFi-6, WiFi-7) and the fact that some spectrum bands are technology neutral. Less expensive and complex solutions will enter the market

3.2.3.5. Identified key strategic actions

The European strategic position given above rsults in the following strategic actions.

Short term (<2026)
• Keep up to date with and validate (private) 5G URLLC systems (trials, testbeds) • Create incentives to further stimulate openness, from O-RAN down to communication chips, stacks and modules • Launch EU funded collaborative RIA projects targeting industry grade communication systems and solutions, stimulating cross-disciplinarity • Invest in strong involvement of SMEs in understanding, benchmarking and trialing various industrial connectivity options • Define a consistent EU spectrum policy, considering licensed and unlicensed and global and local licenses • Define a strategy to enable European manufacturing of industry-grade communication chips • Create incentives to attract students to end-to-end system design programs (from low-level analog to high-level application software) complementing theoretical skills
Medium term (2026-2030)
• Attract investments to enable European manufacturing of industrial communication chips • Grow ecosystem on open reference designs for industry-grade communication • Continued investment in education and training of graduate and post-doc students to bring back essential skills in Europe, that have been lost due to outsourcing • Develop prototypes of industry grade connectivity using 6G innovations

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Long term (>2030)
• Sell fully-EU (from components to systems) industry grade communication solutions to outside EU • Deployment of 6G industrial communication solutions in EU

3.2.4. Recommended general actions for connect and communicate

Europe can gain a strategic position in the HW evolution for 5G and future 6G and has a high potential to lead the technology advances in the mid and long term thanks to the strong knowledge and procurement of talents conducted by European academy institutions and leading industry players in the telecommunication world.

However, the unfortunate combination of the COVID pandemic, climate change, geopolitical tensions, and concomitant supply chain disruptions has increased the demand for semiconductors and a consequent shortage of chips.

In 2020 the major European economies were entering COVID-related lockdowns. Several sectors registered sharp and unanticipated surges in demand during lockdown but not Telecommunications. The positive trend for the telecommunication market risks being affected by the rising demand for semiconductors and the heavy reliance on imported semiconductors materials makes the running situation even worse.

The long-term evolution of semiconductor procurement cost strongly influences Europe's position in the Telecommunication market in the mid and long term. The potential of organizing valid and numerous ecosystems in Europe among system and technology suppliers, medium and small enterprises and local governments can mitigate the risk. The ecosystem can boost the current technology trend and allow the European market to gain critical mass to influence the world market of semiconductors and lower the rising costs linked to procurement of materials for the needed technology step forward both in optics and electronics. The following opportunities can be considered:

- A strong increase of the number of connected devices as Europe rolls out the 5G technology and then 6G.
- Increase of incentives from European governments to establish new fabrication plants if the ecosystems roadmap visualizes for the long-term evolution.
- Foreign investments to expand the growing facilities all around Europe. Competition with outer Europe manufacturing hubs can be faced with more solid strategy plans.
- Reduction of dependencies in supply chains: today, we see a shortage of microelectronics components like in the car industry. This impacts the potential economic growth and recovery in Europe. This observation, together with geopolitical uncertainties, a more regional distribution of suppliers would be beneficial to relax today's dependencies. Such diversity would give more decision freedom to Europe and enable Europe to put its own accents like free and rule-based trade and open markets. With ongoing activities in Europe in the microelectronics domain like a better understanding in the political domain on the strategic importance of the sector, the planned IPCEI 2.0 on Microelectronics and Connectivity, the European Chips Act and potential establishment of new fab(s) from international vendors in Europe (example Intel), there are opportunities in Europe to reduce dependencies by 2030.
- An increase of mutual dependencies between regions in different parts of the value improves opportunities for own decisions in Europe. Mutual dependencies means that no single region is able to support the complete microelectronics ecosystem. Leading-edge microelectronics vendors, e.g., in Asia need to rely to suppliers from Europe for manufacturing machines like lithography. Today, US companies are dominating

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microelectronics design. In this sense there are mutual dependencies. However, the overall European share in this ecosystem is too small and Europe, especially the users of microelectronics (e.g. car industry) are very much dependent. In this relation Europe today is not powerful enough and needs to build up a bigger share in the overall ecosystem. If Europe is able to do this and gets more share in mutual dependencies, Europe has an opportunity in this game. Mutual dependencies also support free trade and open markets, because each player also needs goods from others and may be more willing to follow a rule-based approach.

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Specified impact: short term (<2026), medium term (2026-2030), long term (>2030), undefined

Strengths

- Sizeable indigenous market with strong industrial and automotive actors
- European leaders in wireless infrastructure and industry-grade solutions, from large enterprises to dynamic small enterprises
- High-quality education, strong analog IC design competences
- Presence of leading suppliers of mature and derived IC technologies such as SiGe BiCMOS and SOI
- Much know-how — industrial + research — on packaging, 2.5D/3D integration
- Strong research on very advanced logic technologies ("2nm CMOS" and beyond) and RF devices (GaN, InP)
- Strong in front-end modules for UE
- Industry 4.0 vision originated in EU and further being developed e.g. 5G-ACIA)
- Several photonic platforms in EU
- EU is preparing for 6G via several initiatives (SNS, flagship, Horizon Europe, NetworldEurope, ...)

Weaknesses

- Loss of expertise in IC design due to outsourcing in the past
- No big players left in wireless UE products/chips and in optical comm chips/components
- Ecosystems related to microelectronics are drying up in EU
- EU presence in solid-state design and technology conferences decreasing
- Heavy dependence on imported ICs (electronics and photonics)
- RF & mm-Wave IC design know-how increasing, but to be improved yet
- Less engineer students graduating with knowledge on analog/digital/RF IC design and complete end-to-end systems (from analog to high-level application software)
- Limited spillover from research to industry (e.g. in integration technologies)
- Huge investments needed for design and fabrication of advanced logic chips
- No large commercial European fabrication chain for InP
- Global spectrum licenses limit competitiveness in industrial grade connectivity

Opportunities

- Explosive growth of wireless market expected
- Getting worldwide market leadership in 5G/6G wireless backhauling and FWA
- Mm-wave and sub-THz bands need new TRX architectures with beamforming and advanced heterogeneous integration
- Speed of CMOS saturating, opportunity for SiGe BiCMOS, InP
- Strong push for energy efficiency beneficial for use of very advanced CMOS in digital and non-CMOS technologies for generation of transmit power
- Complex front-end modules will require advanced heterogeneous integration
- Complexity in digital baseband increases a lot
- Increasing attention to openness (e.g. O-RAN) to enable faster innovation
- more incentives from EU government to establish new fabrication plants
- foreign investments to expand the fabrication facilities all around Europe.
- Reduction of dependencies in supply chains
- Mutual dependencies between regions in different parts of the value chain should be increased to improve opportunities for own decisions in Europe

Threats

- Photonic and Electronic chip shortage
- Market evolution uncertainty due to COVID, climate change, geopolitical tensions
- Non-EU competitors have very aggressive product portfolio and expertise, making high barriers to entry
- Dependence on non-EU providers of components
- Standardization dominated by few big players, including non-EU competitors, introducing barriers to entry
- Failure to attract and educate engineers within EU
- Design and processing in advanced logic processes expensive
- Network operators may have potential cash problem to improve the network, reducing the volume, thus ROI
- Societal opposition: 6G consumes too much energy, advanced features not widely accessible
- Expected 6G volumes go beyond worldwide installed capacity of non-CMOS technologies
- Competition from other regions (6G, foundries, front-ends, ...)
- Undefined standardization and uncertainty on future requirements on 5G and beyond network can determine loss of R&D investment

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3.3. EG3: sense and power

The goal of Expert Group 3 (EG3) is to identify key challenges for innovations in the areas of sensing and power for future networks. EG3 identifies key technologies and strategic actions that enable Europe to build trustworthy and competitive solutions in the four market segments addressed by COREnect:

- Connectivity Infrastructure
- Consumer Grade Connectivity
- Industrial Grade Connectivity
- Automotive Connectivity

This expert group explores the challenges and opportunities that are going to confront not only the telecommunications and microelectronics industry, but the whole value chain and society. 6G will enable completely new services to consumers, e.g. digital health with wearables and on-body sensors. This allows unprecedented opportunities (e.g. for better diagnosis) as well as societal threats. EG3 suggests areas for strategic action to favor acceptance and usage of the new opportunities, as well as ensuring European sovereignty in the new technologies needed.

Future connectivity systems for all market segments hinge on a reliable infrastructure and novel, distributed sensors that generate a huge amount of data. This pushes the frontiers for edge preprocessing, energy-efficient connectivity, low latency communication, cloud computing and AI.

3.3.1. Connectivity infrastructure

Figure 18 describes the market sub-segment, applications, power management requirements, core process technologies and system requirements. The focus thereby is on massive data collection and transfer, AI/ML integration and the integration of sensing and communication capabilities in future infrastructure. These refinements were addressed to define the European strategic position and the suggested key strategic actions.

<table>
<tr><th>Market segment</th><th>Applications</th><th>Power management</th><th>Core process technologies</th><th>System Architecture</th></tr>
<tr><td>Sub 6 GHz bands</td><td rowspan="2">Wireless basestations 5G</td><td rowspan="3">Higher efficiency for lower power dissipation</td><td rowspan="3">SiGe and RF Packaging</td><td>SoC with Speciality RF amps</td></tr>
<tr><td>mmWave 5G</td><td rowspan="2">SoC with speciality RF frequency converters, analog signal processing and amps</td></tr>
<tr><td>mmWave 6G</td><td>Wireless basestation 6G</td></tr>
<tr><td>mmWave 6G</td><td>RADCOM (ISAC), RF components</td><td>Higher efficiency for lower power dissipation</td><td>RF components & technologies, RF packaging/modules</td><td>RF SoC & packaging, SW defined radio</td></tr>
<tr><td>sub 15 GHz für 6G</td><td>Wireless basestations (5G, 6G)</td><td>Higher efficiency for lower power dissipation</td><td>RF components & technologies, RF packaging/modules</td><td>SoC with Speciality RF amps</td></tr>
</table>

Figure 18: Refinement of the connectivity infrastructure market segment.

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3.3.1.1. European strategic position and potential - SWOT

The discussions within this market segment resulted in splitting the SWOT analysis in (1) semiconductor technology and (2) RF packaging.

European strategic position on semiconductor technologies:

Strengths	*Weaknesses*
• Strong base in EU over multiple companies (ST, NXP, IFX) and ODM (Ericsson, Nokia); Bosch • Key equipment supplier from EU (ASM, ASML, Besi, SPTS, EVG, Boschman, ….)	• Industrial base for expansion in Taiwan and China • RF ICs design process is low automated (analog vs. Digital design tools) • Consumer electronic reference design makers (Qualcomm, Broadcomm, Intel) US based
• EU based Fab • AI support from chip to system • Governmental support on speed up of frequency allocation for communication (Wifi and 6G) • Hands on support to enable green transition	• Slow decision and scattered interests of member states • Fragmented specialty RF field makes investment risky • International companies impacted by US bans • Tough competition due to large size of subsidies in China and USA (Darpa) on manufacturing process
Opportunities	*Threats*

European strategic position on RF packaging:

Strengths	*Weaknesses*
• Patent position • Strong institutes (FHG, Imec, TNO, CEA Leti) • Industrial base (PINS, AMKOR Portugal, Sencio, …) • IC companies (users) with package knowledge	• Industrial base of OSATs (and eco system) dominated by Far East • ODMs industrial base is limited in EU • Industry has volume and price focus over innovation and location of production • Limited university grades in packaging
• Increasing complexity requiring high end packaging (to be brough in volume at consumer prices) • Use regulations to shape this industry to be compliant with long term green & human goals of EU • EU subsidy program to focus on EU strategic development	• Tough competition due to large size of subsidies in China and USA (Darpa) on manufacturing process • Slow decision and scattered interests of member states • Big Tech is US/Pacific oriented
Opportunities	*Threats*

3.3.1.2. Identified key strategic actions

Short term (<2026)
• Define policies - copy China way of working - sell in EU = make in EU • start education of right people in right amount • Use labor available in eastern/south EU to build up infrastructure for assembly
Medium term (2026-2030)
• Execute, strengthen and adjust policy
Long term (>2030)

3.3.2 Consumer Grade Connectivity – Consumer Healthcare

Digitalization enables heath monitoring equipment to be compact and portable, which opens opportunities for consumer healthcare This is clearly illustrated in Figure 19 [Yol20]. In the

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transformation of healthcare organizations, the COVID pandemic will probably accelerate technology requirements toward a patient centric approach: more telehealth, more wearable, hearable and connected medical devices & more prevention through continuous monitoring.

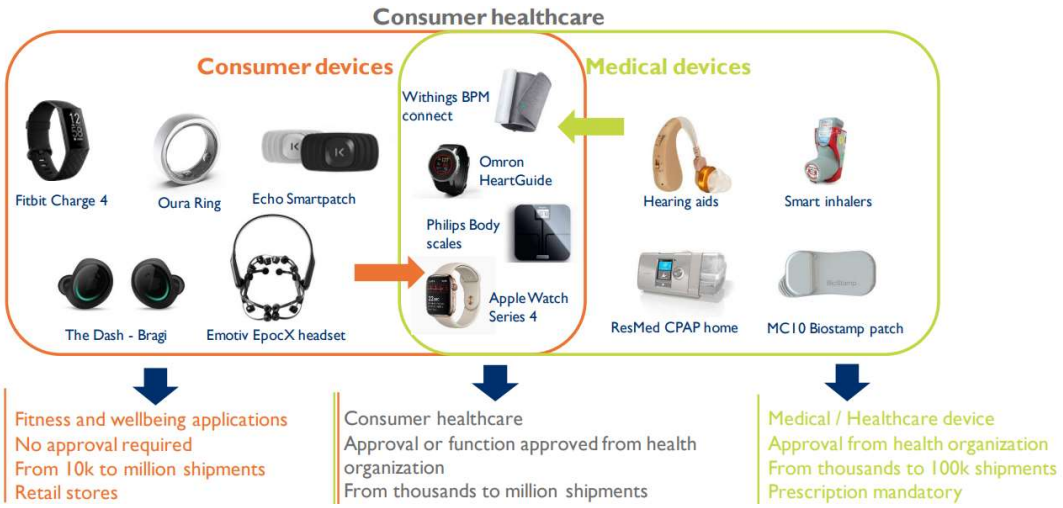

Figure 19: Consumer healthcare is a new application domain, emerging from fusing consumer electronics with medical devices [Yol20].

The integration of 6G will revolutionize the way health monitoring and healthcare will be solved. An important example is the potential use of 6G technologies for supporting extremely low-latency healthcare data transmission and accelerating medical network connections between wearables and remote doctors [Ngu20]. An overview on the performance improvement from 5G to 6G is shown in Table 3.

Table 3: Expected performance improvement from 5G to 6G [Ngu20].

	5G-IoT	6G-IoT
Data Rate	20 Gb/s	1 Tb/s
Mobile Traffic Capability	100 Mb/s/m²	1 Gb/s/m²
Connectivity Density	10E6 devices/km²	10E7 devices/km²
Network Latency	1 ms	10-100 µs
Coverage	70%	>99%
Energy Efficiency	1000 x 4G	10 x 5G
Spectrum Efficiency	3-5 x 4G	>3 x 5G

Many remote systems in the healthcare domain, e.g., remote health monitoring, remote surgery, and haptic application require low latency communications (below 1 ms) with the reliability requirements of above 99,999%. 6G robotics can be applied to implement remote surgery in a fashion that remote doctors can manage the surgery via the robotic systems in the context of 6G at a latency of milliseconds and high reliability. The ultra-low network latencies (10-100 µs) fulfill the requirement of haptic applications such as e-health and autonomous driving. A telesurgery system in the context of 6G, UAVs and blockchain is studied in [Gup21]. Due to the use of blockchain technology, each robot acts as a data node so that surgical information is stored securely in the database ledger without the need of centralized authority. Accordingly, wearables, on-body sensors, implants, and nano-sensor-devices can communicate and transmit data in real-time with extremely high reliability and availability to edge devices or cloud centers for preventive- short and long-term medical analysis. 6G-based URLLC (Ultra

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Reliable and Low Latency Communication) has been exploited to facilitate connected ambulance in future healthcare, by allowing real-time video streaming with high color resolution for reliable diagnosis to clinicians and paramedical staff from the hospital at moderately high speeds. An overall picture of the vision of future 6G based IoT applications is illustrated in Figure 20.

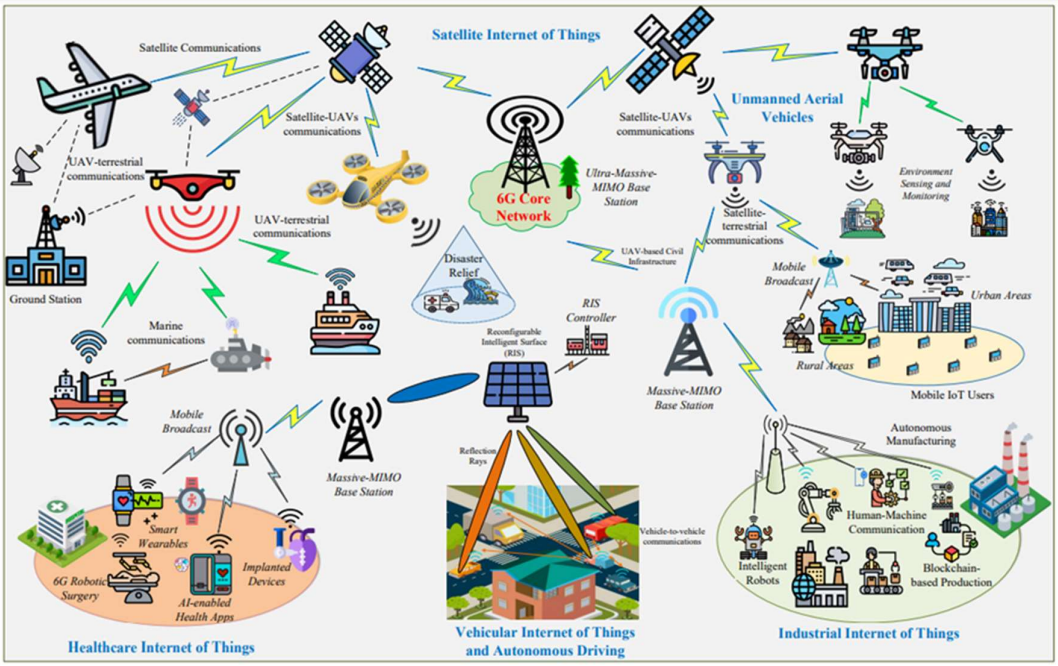

Figure 20: Vision of future 6G-based IoT applications [Ngu21].

The integration of blockchain and MEC (Mobile Edge Computing) with its decentralization, immutability, and traceability features potentially offers high degree of security and privacy to healthcare operations, e.g., secure Electronic Medical Records (EMRs), in the digital healthcare era, it is of utmost importance to share EMRs across healthcare institutions to support collaborative health services and achieve universal healthcare [Ind20].

Another opportunity is to adopt edge cloud computing to provide low-latency health data analytics for healthcare services such as diagnosis, disease prediction, and intelligent decision-making tasks for physical medicine and rehabilitation. In this context, ML is also useful to optimize mobility management processes by taking data rates, traffic flows, data processing delays, and bandwidth resource allocation into account. Implementation results show a good trade-off between time and energy efficiency by using ML techniques while effectively managing and monitoring the mobility of the IoT driven devices in 6G-empowered industrial applications including healthcare services. Recently, COVID has spread rapidly across the globe and become a major health concern of many countries. Wireless and wireline communication technologies such as URLLC, edge intelligence, and cloud computing have been applied to combat the COVID pandemic in different ways. In future a regularly and online monitoring with Intelligent Wearable Devices (IWD) will increase the efficiency and quality of the public health system dramatically.

Intelligent wearable devices will be connected via 6G to the Internet and transmit physiological and physical data to test centers and monitoring centers. These devices will monitor heartbeat, blood pressure, blood tests, health conditions, body weight and nutrition. The test result will be received quickly. Also, IWD learn from the personal body history and advise the person for the

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next action, for instance, advising for walk or running. IWD will maintain a personal history of health, nutrition, and habits. Thus, IWD can advise what to eat in case of any deficiency. Detection of minor body issues such as deficiency will reduce the frequency of hospital visit [Nay21].

3.3.1.3. Short term impact (<2026)

The rising prevalence of chronic conditions (diabetes, obesity…) and the outbreak of COVID are key drivers for the market. There is a growing demand for point-of-care testing devices. Governments are supporting fast-track approvals for new products.

3.3.1.4. Medium term impact (2026-2030)

Rapid technological advancements are expected to be a significant factor for market growth. COVID breathe analyzers, currently under clinical validation might hit the market [Wal21]. New biz models will appear with medical equipment manufacturer growing into data service providers (Medical Edge). Data storage will require high security level. KI in medical edge will allow remote maintenance.

3.3.1.5. Long term impact (>2030)

With climate change the risk of new pandemics is predicted to increase. Further market growth for point-of-care testing devices can be expected after security concerns are addressed.

3.3.1.6. European strategic position and potential - SWOT

This section contains a translation of the descriptions above into a SWOT analysis.

Strengths	*Weaknesses*
• COVID breath analyzers from EU Companies (Imspex diagnostics, Wales; Breathomix, Netherlands; RAM Group, Germany) • Big players in EU (Siemens AG, Philips, …) • Trustworthiness is European domain • Advanced electronic sensors and photonics, MEMS • Low-cost mass production • European strength in robotics	• Market is fragmented, many small players with distributors (non-European) • Distributors might not be trustworthy (in case of chip shortage low priority on security) • Slow innovation; point solutions and low volume; strict regulation • Borders between Pharma, MedTech & ECS (Electronic Components and Systems industry) • Quite a distance to competitors in advanced CMOS nodes • IA chips for healthcare wearables
• Strong market growth due to nanotechnology based bio-sensors, molecular biology • Open technology platforms, shared standards • Consumer healthcare to penetrate medical market • Remote surgery with high end robotics will get more important	• Distributors in Hongkong, China, US might dominate the market • Apple/fitbit etc. advantage in big data collection & handling
Opportunities	*Threats*

3.3.1.7. Identified key strategic actions

Short term (<2026)
• Create acceptance for sensitive data sharing, online monitoring with wearables • Supply chain overarching activities (industry alliance) • Standardization for lab on a chip, PCR (point of care) - molecular biological diagnostics • Set up eMR (electronic medical record)

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Medium term (2026-2030)
• Build AI on top of eMR • Investment, funding • Security, standardization • Imaging needs high processing power
Long term (>2030)
• Further develop AI for eMR

3.3.2. Industrial Grade Connectivity

In the vision of ambient intelligence, the ability to gather detailed and accurate information is key and relies mainly on smart intelligent sensors able to measure and communicate. Numerous studies envisioned several billions of sensors, tags and small IoT devices in next few years.

However, it appears that the need to power those devices through batteries or main AC power is a key limitation for their deployment, mainly for cost, operational and environmental constraints. Therefore, the ability to produce battery-less devices, able to extract the power they need from their environment is crucial to enable the wide deployment required by a highly efficient environment. This will have implication on the industrial applications (logistic, building automation, smart cities, ...) and on the consumer market.

Not only does it require to develop energy harvesting capabilities (solar, electromagnetic field, heat, vibration...) but it also implies to both develop extremely power-efficient electronics (MCU, sensing, analog, RF, power management) on one side, and an expertise on energy-efficient software coding on the other side.

We focus here on key technologies required to support new generation connectivity in industrial markets. When looking at industrial sites, the main applications in focus are industrial grade wearables, IoT for remote machine control and smart metering, ultra-wide bandwidth sensors and gesture recognition. However, the same technologies find broader usage in modern agricultural sites, smart cities, smart homes and smart buildings with very similar and sometimes worse constraints in performances.

The diversity and complexity of new connectivity requirements are driving businesses to review their strategy and seek new solutions.

Public cellular networks do not give the local control and flexibility required in private networks in the way that Wi-Fi does. On the other hand, Wi-Fi is not designed to cover large areas, connect large number of devices or to be used for critical communications.

5G networks are a new standard capable of responding to new needs and offering hitherto unimaginable opportunities for industry and society.

One of the main fields with large innovation potential is IoT technologies employed throughout all industrial activities from production to transportation, logistics and retail. Wide adoption of IoT technologies is possible only with industrial grade connectivity. Beside smart sensors used on the factory's floor to control and monitor production, for low latency human-to-machine and machine-to-machine communication, smart wearable devices represent the next step to improve productivity. AR Glasses, VR Headsets, Smartwatches, Smart Bands are some examples of smart wearable electronics, used not only in tasks like package handling, truck loadings, tasks

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in warehouses and production lines, retail and transportation operation, but also to ensure employee's health by monitoring posture, movements and for remote assistance and training.

Smart farming and digitalization of the agriculture are already a strong focus of the European community. IoT sensors collect environmental and machine data, which farmers can exploit to make better decisions as well as to improve every aspect of their work, such as crop farming and livestock monitoring. Indoor farming and aquaculture among other aspects greatly benefit for deployment of smart sensors and improved connectivity. Combination of IoT real-time data with accurate geo-spatial data is the key enabler of truly precision farming.

The COVID pandemic, mounting decarbonization commitments, resource constraints and continuous urban growth are making a new case for making the cities smarter, more efficient, and sustainable for their residents.

Considering that cities consume over two-thirds of the world's energy, the need to reduce the carbon footprint requires adoption of key technologies like smart grids, micro-grids to use and share local energy sources, next-generation energy transmission, distribution networks with automatic monitoring of energy flows and adjustment to changes in supply and demand.

It is clear these innovations require changes to urban infrastructure and accelerated deployment of new technologies including 5G, AI, cloud, and edge computing is helping to drive the evolution of Smart Cities, with IoT sensors distributed all over the city's territory. The extended connectivity drives the need for high reliability and security of the network. This makes it necessary for telecom and technology companies to collaborate among themselves and with government and invest in reliable networks, cybersecurity, and backup systems.

Decarbonization can be addressed not only at city level but also down to buildings and house levels. Commercial buildings account for 20% of energy use in the US, 30% of which is wasted. Smart solutions pave the way to make them energy-efficient and sustainable, whilst automated management allows expansion of the building's nervous system into a network of smart buildings.

Key elements of this transition are smart sensors, which generate detailed, real-time data about the building, from occupancy to ventilation, lighting, and power demand. Smart buildings should be capable of adjusting their power consumption in real-time communicating with the city's grid and using local storage elements. For example, excess heat produced by office buildings can be transformed into locally stored energy, which can be used in case the grid requires temporary reduction of the energy consumption.

One of the fundamental topics to be addressed is how to manage power of all these sensors and how to handle the huge amount of data generated by them.

3.3.2.1. Short term impact (<2026)

At short term, solar powered devices are likely the first to be mature enough to enter a large market as prototype of solar powered Bluetooth enabled sensor are now state of the art. However, to be able to enter the consumer market, some progress is still required in terms of cost (ultra-low power is expensive) and reliability. Most early application will likely be on building automation

Widespread use of IoT device and sensors generate a huge amount of data. Direct transmission of this amount of information is not feasible and contributes to the power demanded for the

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communication. One key technology which helps reducing the amount of transmitted data is AI pre-processing. An edge AI processor embedded in the sensor identifies the useful information to be transmitted, therefore reducing the required rate. Due to the intrinsic discontinuous nature of IoT sensor operation, neuromorphic circuits allow minimum power consumption. Memristor based analog or mixed-signal AI processors do not require large amount of digital processing, therefore huge investment in small IC technology nodes is not necessary.

Moving to smart buildings and homes, high voltage direct current (HVDC) buses provide the possibility to reduce power consumption and to adopt smart power management solutions thanks to the availability of power converters and metering sensors. High density and high efficiency are key parameters for such systems and wide bandgap devices (WBG) are necessary to boost the performances. Target is to strengthen the European position in wide bandgap devices exploiting the know how built so far by many European companies.

AI technology not only supports large deployment of IoT devices but is also fundamental for the management of telecommunication and power grids. By properly monitoring the network, AI processors can consider large number of variables and optimize the performances despite the high level of complexity. Edge AI processors rely on small technology nodes, which are not readily available in Europe. Short term target should be strengthening collaboration with companies outside Europe on one side, while on the other side it is necessary to create a solid know-how on how to implement suitable algorithms for these tasks. Machine learning, neural network training and training dataset identification are some of the key critical intellectual properties needed.

3.3.2.2. Medium term impact (2026-2030)

Lower cost of energy-harvesting function and more efficient ultra power components open the gate to widely disseminated battery-less communicating devices, even for “almost disposable” usage (ex: parcel tag) allowing European companies to take advantage of a much more efficient supply chain, logistic and shipping capacity thanks to the various optimization powered by those smart tags.

3.3.2.3. Long term impact (>2030)

Universal energy harvesting devices are able to use jointly different energy sources so that they are able cope with every situation and be reliable enough to replace support critical services (roadside infrastructure for ex.)

As sensors shrink in size and use optimized technologies which reduce power consumption, integration of micro batteries onto ICs extends the lifetime and processing capabilities of the devices. The main challenges to be resolved for adoption of micro-batteries are related to manufacturing and compatibility between conventional IC process and materials used by micro-batteries. Also, further research is necessary to overcome the limited energy density of this type of batteries.

This opens a lot of perspective towards a fully automated fab and intelligent personal as well as industrial robotics applications, leading to much better working conditions for humanity. Also in mobility, it will lead to a zero-accident world with much less traffic congestions.

3.3.2.4. European strategic position and potential - SWOT

This section contains a translation of the descriptions above into a SWOT analysis.

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Strengths	*Weaknesses*
• Big player in ultra-low power component (STM, CSR, Nordic) and in RFID (which is the precursor) • Big player in WBG	• Volumes remains small. Chip production is still done mainly outside EU
• Transaction for autonomous devices will increase in the future for many reasons, including environmental constraint and maybe regulation	• US and Chinese actors are also very active on RF Energy harvesting and China is sensitive to supply chain optimization
Opportunities	*Threats*

3.3.2.5. Identified key strategic actions

Short term (<2026)
• Strengthen the European position in wide bandgap devices • Further regulation, standardization for authentication, encryption (data space connector factory --> internet) • Funding start-ups • Develop AI cores for edge sensors • Further research on Si batteries, integrated batteries, energy harvesting technologies, micro solar panels • Improvement in wireless charging
Medium term (2026-2030)
• Improve AI cores for edge sensors • Improve localization for IoT in an industrial context • Further research on HF communication; alternative solutions for power distribution • Further research on optical communication
Long term (>2030)
• Further research on power over fiber

3.3.3. Automotive connectivity

Automotive connectivity is evolving very rapidly. Whereas in the past a vehicle consisted of ''connectivity islands'', the vehicle is now more and more evolving towards an integration of mutiple type of connectivity standards, both internally in the vehicle as well as outside the vehicle to the external world (environment, infrastructure, other vehicles and other road users). One important element is the evolution from ADAS (Automated Driving Assistance Systems) to fully autonomous vehicles. Another example according to research by IOT Analytics, is ''Traffic Monitoring & Management''. Sensing thereby will have to become a feature offered by the network including all kinds of spatial monitoring. Thereby different types of radar and other sensing elements will have to be integrated with communication and connectivity networks and devices.

Figure 21 describes the applications, core process technologies and system requirements for automotive connectivity market segment.

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Applications	Core process technologies	System architecure /system requirement
ADAS - autonomous driving, wireless	FPGAs & ASICS, real time processing of complex data--> MC with AI accelerators --> most advanced CMOS process nodes, neuromorphic computing	"reliability procedures, retransmission or redundancy" - enable selfhealing (software update)
In cabin sensing	> 100 GHz (high resolution, antenna size, interference with 77 GHz RADAR	High resolution imaging with THz, e.g. detection of persons on the rear seat (children) and are they wearing seatbelts
Automotive RADAR: Front facing ADAS applications like automatic emergency breaking, automatic cruise control	77, 79 GHz CMOS/SiGe radar chipsets and companion radar processors	Radar front end with multiple Tx and Rx chip (for imaging radar cascaded front ends) in conjunction with a radar processor
Automotive RADAR: Side facing ADAS applications like blind spot detection, lane change assist	77, 79 GHz CMOS/SiGe radar chipsets and companion radar processors	Radar front end with multiple Tx and Rx chip in conjunction with a radar processor
sensorfusion(radar, ultrasonic, lidar, camera...)		

Figure 21: Defined sub-categories for automotive connectivity market segment

3.3.3.1. European strategic position and potential - SWOT

This section contains a translation of the descriptions above into a SWOT analysis.

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Strengths	*Weaknesses*
• Automotive qualification & design experience to build robust & reliable systems • Design of specialized MCUs • Software tools for FPGA design (Siemens EDA) • For Radar: MMIC in CMOS & SiGe mm-wave design capabilities • Europe is strong in power converter (for connectivity) • Focus on energy efficiency (GaN, SIC available)	• High automotive qualification requirements slow down T2M • Large scale digital chip manufacturing: No highly integrated CMOS designs • No European actor in CPU or FPGA missing semiconductor technology for high frequencies (III/V)
Opportunities	*Threats*
• Design capability • Neuromorphic computing? • Standardization (need participation in the different standards) • For power capabilities: bring server infrastructure into car / calc performance • For higher frequencies, higher performance needs to build on our capabilities for harsh environment • AI based approaches to design process -> T2M acceleration, esp. for V&V	• Competitors from outside automotive community (e.g. Tesla, Google car) • Automotive RADAR EU has no highly integrated CMOS single chip radar system (US only offering) • Radar interference: Digital radar at 77GHz threat to FMCW (wide adoption and EU strength)

3.3.3.2. Identified key strategic actions

Short term (<2026)
• Participation in standardization committees (RADAR) product realization, in the past it was also the other way (RADAR in smart phone) - for level 4 ADAS (Advanced Driver Assistance Systems) • Participation in regulation for frequency spectrum radar > 100GHz for automotive radar • Develop the Strategy for power management in Cars (decentralized, smart power management in the car), battery charge, based on AI, AI processors for edge (CMOS low node) • Go for edge Computing Strategy, which is Suitable to use technologies available in Europe • Solve radar interference with increase of radar adoption in vehicle fleet • Further regulation, standardization, authentication forV2V, V2Xcommunication e.g., C-ITS (collaborative, intelligent, transportation System), ADAS black box
Medium term (2026-2030)
• develop a power strategy for cars (datacenters on wheel), connected with edge computing • Expand radar sensing in higher frequencies (SiGe leads the way, CMOS needs to follow)
Long term (>2030)
• Highly integrated THz imaging

3.4. Common strategic actions across the expert groups

Beyond the technical actions proposed by each expert group, some transversal actions can be defined as key enabler to secure and strengthen the proposed strategy. This section gives a first glimpse on some common strategic actions that can be beneficial to the full connectivity value chain. The final roadmap deliverable (D3.6) will come with a more solid interpretation of the strategic actions described over the different focus areas and market segments.

Note: Expert Groups have also discussed the potential role of SMEs and more particularly the importance of creating incentives that would stimulate startups in microelectronics design. Initial ideas on the potential role of SMEs and recommendations on how to support the emergence of "European champions" in the field of microelectronics and connectivity is

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presented in section 2.2 of COREnect Deliverable 4.2 "Interim report on community building and outreach". This aspect will be further discussed in the coming months within the project, as part of Task 3.2 "Core technologies development recommendations and guidelines" and Task 2.2 "R&I and investment requirements for developing European core technologies in 5G and beyond" and shall be an integral part of Deliverable 3.6 "Final COREnect industry roadmap".

3.4.1. Maintain & strengthen Europe on semiconductor manufacturing equipment to have some leverage on its capability to access key non-European technologies

As mentioned previously, semiconductor manufacturing equipment has played a key role in the ability of USA to prevent China to access to key semiconductor technologies (while not owning the associated manufacturing capability). To avoid Europe to encounter similar issues, it is key that Europe increasingly protects and strengthens its assets. As such, Europe has some leverage if global trade tensions escalate further. It would also enable Europe to speak on its own rather than being forced to pick sides. A dedicated R&D program supported by the European Commission in addition to IPCEI and KDT could be dedicated to support the Europe semiconductor ecosystem to maintain its position and build strong collaborations with other countries (for example Japan and South Korea).

3.4.2. Strengthen Europe's position on EDA solution market

EDA vendors are also playing a key role in the current trade tension and strategy deployed by USA. Today, the USA is the key semiconductor EDA solution provider (Cadence and Synopsys) but Europe has the potential to have a strong contender (e.g. Siemens EDA). Consequently, it is vital to strengthen this asset to secure Europe's sovereignty to access key technologies and to prevent European industrial players to be locked in a monopoly. Dedicated actions targeting to revitalize Europe's start-up ecosystem on EDA solutions could be one approach.

3.4.3. Support Europe's contribution to standardization activities

Standardization is playing a key role on the capability of industrial players to capture new market opportunities and to operate on wide and open markets. The way Chinese players have been pulling resources on 5G standardization and the impact it had on the value captured by Chinese players (such as Huawei) on the 5G market is a very good example. Notably, the first response of China's Ministry of Industry and Information Technology to increasing trade tension with USA was to announce the creation of a semiconductor standards committee composed of 90 leading Chinese companies. It is advisable that Europe acts diligently by, for example, providing tax incentives to companies allocating financial resources and dedicated staff to standardization activities. This could help to ensure that Europe plays a sufficient role on this topic. Another means are tax benefits for research in Europe to develop necessary standards essential IPRs, which will be implemented in global standards.

In the framework of COREnect it is important to stimulate research programs that accelerate the knowledge transfer from universities and institutes to the European semiconductor industry (as well as joint research) that generate technologies and innovations implementing the 3GPP-standardized URLCC features in the short term. Wireless sensor networks should not rely only on 5G-RAN to reach highly reliable low-latency capabilities. Also, the focus of governmental efforts and research institutes should be further set on URLLC over other RAN, e.g., WiFi or UWB, and help to close the standardization gaps. Consequently, in the future, the different technologies can be integrated in a wide interoperable network that allows seamless, secure,

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low-latency and reliable interaction of sensors and IoT devices, independent from the RAN technology.

The vision for 2030 must be the European semiconductors industry and public institutions enabling a non-centralized communication network, in which every node and end devices (e.g., sensors, controllers, actuators, HMIs and the like) can guarantee reliable and secure communications according to the QoS demanded by individual markets (e.g. automotive and autonomous driving, industrial IoT and TSN), RAN-technology agnostic, and always oriented to satisfy end user and environmental requirements.

3.4.4. Strategic Infrastructure program lead by state members and the commission

Europe has wireless infrastructure players (Ericsson and Nokia) able to compete with Chinese ones (Huawei and ZTE). Still, in 5G deployment and associated value creation through new services, today Europe is lagging behind. In the NB-IoT market, for example, China accounts for 92% of the global NB-IoT connections. This is the result of the clear and aggressive deployment objective which was set by China's Ministry of Industry and Information Technology concerning NB-IoT. It enabled Chinese IoT hardware vendors to leverage their domestic market to develop their chipset solution. Cost-effective solution and deployed infrastructures being available, key verticals have then leveraged this asset to create high-value services addressing key societal challenges. As such, a clear and ambitious deployment strategy for an investment-friendly environment of 5G and 6G networks at the scale of Europe, as well as state funded infrastructure deployment program especially in areas which may not be served from purely economic reasons (as it has been done in France for optical fiber access), would clearly help to make sure that Europe can build its future leadership on connectivity technology on a solid foundation. States can also play the role of early adopters for public services to stimulate investment in public infrastructure for citizens. This suggestion also applies to cloud infrastructure to strengthen Europe's position on this market and enable a European ecosystem to emerge.

The European Commission promotes Green Digitalization and high standards in privacy and security. This offers opportunities to focus European research but also European regulations and certification procedures in aligned directions which both benefit the European goals but also the European industry.

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4. Conclusion

This report consolidates the COREnect's initial views on the strategic R&I roadmap for future European connectivity systems and components. These views have been structured around three key strategic focus areas and four market segments to maximize the social and business impact potential. These views are defined based on input from relevant stakeholders by the installation of expert groups. These expert groups have been divided over the COREnect strategic focus areas: (1) compute and store, (2) connect and communicate, and (3) sense and power. The following market segments have been applied over these strategic focus areas: (1) connectivity infrastructure, (2) consumer grade connectivity, (3) industrial grade connectivity, and (4) automotive connectivity. For each of these market segments, SWOT analyses are presented, and related strategic actions are proposed in this report. These results are mapped onto a timeline to create impact. This timeline covers the short-term impact (<2026), medium-term impact (2026-2030) and long-term impact (>2030). At a glance, the defined strategic actions for Europe focus on strengthening its semiconductor manufacturing equipment, strengthening its position in the EDA solution market and fabless actors, safeguard its needed skills and expertise, enhance its contribution in standardization and maintain its support to strategic infrastructure programs.

This report is the second in a series of three. This report prepares the upcoming work to derive global/common COREnect roadmaps and strategic actions across value chains and focus areas. The current report leverages and complements the input and insights provided by the relevant stakeholders and introduces a common structure in each of the focus areas. This common structure, building around a discrete set of market segments, paves the way to define a final strategic roadmap report D3.6 with a high business and social impact potential. Moreover, the current report sources the activities in T3.2 to define actionable recommendations and guidelines for relevant private & public stakeholders and to raise their awareness of the required investments.

Given this buildup, it should be clear to the reader that the current report (D3.4) is the second to last step in defining the envisioned strategic roadmap.

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6. Appendix

The COREnect roadmap activities strongly rely on interactions with experts in the field. Some of the current members of the COREnect expert groups, as described in Section 3, are listed below.

Experts from within the consortium (non-exhaustive list):

Barkhausen Institut GmbH	Michael Roitzsch, Sebastian Haas
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IIIV/Nokia	Mohand Achouche
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Nokia Bell Labs	Volker Ziegler, Wolfgang Templ, Patricia Layec
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