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List of Abbreviations

Abbreviation	Denotation
5G	5th Generation of wireless communication
5G PPP	The 5G infrastructure Public Private Partnership
6G	6th Generation of wireless communication
AI	Artificial Intelligence
ASIC	Application Specific Integrated Circuit
BCG	Boston Consulting Group
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CAD	Computer Aided Design
CAGR	Compound Annual Growth Rate
CMOS	Complementary Metal Oxide Semiconductor

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CPU	Central Processing Unit
EC	European Commission
ECS	Electronic Components and Systems
ECSEL	Electronic Components and Systems for European Leadership
EIB	European Investment Bank
EIC	European Innovation Council
FEM	Front End Module
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GPU	Graphics Processing Unit
IC	Integrated Circuit
ICT	Information and Communications Technology
IDM	Integrated Device Manufacturer
III-V	Semiconductor with elements from groups III and V of the periodic table
InP	Indium Phosphide
IoT	Internet of Things
IoX	Internet of X
IP	Intellectual Property
KDT	Key Digital Technologies
MCU	Microcontroller Unit
ML	Machine Learning
mMIMO	Massive MIMO (multiple input, multiple output)
OEM	Original Equipment Manufacturer
O-RAN	A disaggregated and virtualized RAN, spearheaded by O-RAN Alliance
OS	Operating System
R&I	Research and Innovation
RAN	Radio Access Network
SDG	Sustainable Development Goal
SiGe	Silicon Germanium
SME	Small and Medium-sized Enterprise
SNS	Smart Networks and Services
SoC	System on chip
UN	United Nations

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VC	Venture Capital
WP	Work Package (of a project)

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1 Updated Vision on European priorities of micro-electronics towards 6G

In the advent of an intelligent and connected world, the underlying, enabling technologies have made headline news. Modern societies' dependence on semiconductor technologies, microprocessors, and system-on-chip (SoC) has become painfully obvious in a very short time. In parallel, the evolved digital infrastructure and related technologies are becoming undisputable cornerstones for economic development. Like roads, power grids and other basic infrastructure that once propelled societal development in the 1900s, digitalization will do the same for this century. However, the roads towards future, sustainable prosperity are not made of asphalt – they are spelled waveguides, photonics, wireless and silicon.

Everything benefitting from being connected will be connected as part of the IoX (internet of everything) mobile revolution. While 5G is rolled up globally, standardization for its future is already taking place for what is today commonly named 5G-Advanced (5G-adv) with 3G-PPP release 18-20 targeting among others personal IoT networks, cloud gaming, enhanced sidelink, accurate positioning, etc. Meanwhile, visions, use cases and disruptive key technologies for a possible 6G system are extensively discussed and research efforts are baked. Publicly funded 6G research projects in Europe, the United States, and China are under way, and also the ITU has begun its work on requirements for fixed networks in the 2030s. Such vision could be summarized in 6 theme including new spectrum technologies, extreme networking, RAN-Core convergence, security and trust, network as a sensor and AI/ML air interface. A common theme in many 6G vision papers is that of creating digital twin worlds for seamlessly connecting and controlling physical and biological entities to enable new mixed-reality super-physical experiences and in the meanwhile addresses major societal challenges with sustainable, trustworthy and inclusive design. As a result, connectivity solutions of today and tomorrow such as 5G and 6G will enrich all product segments and create added value for consumers - but is the European ecosystem and in particular microelectronics equipped to embrace and capitalize on this transition?

Since 2000, we have seen a changing landscape in the semiconductor industry, which has been in full transformation, a transformation which is still on-going, as depicted in the picture below. Today, Europe is positioned close to the end customers with a large relative footprint for end-user equipment and related services as shown in the following figure. The percentage is much smaller for electronics and embedded systems. When added value is created thanks to connectivity and software, there is a large risk that Europe's share of the total added value will be diluted and shifted to areas dominated by other regions.

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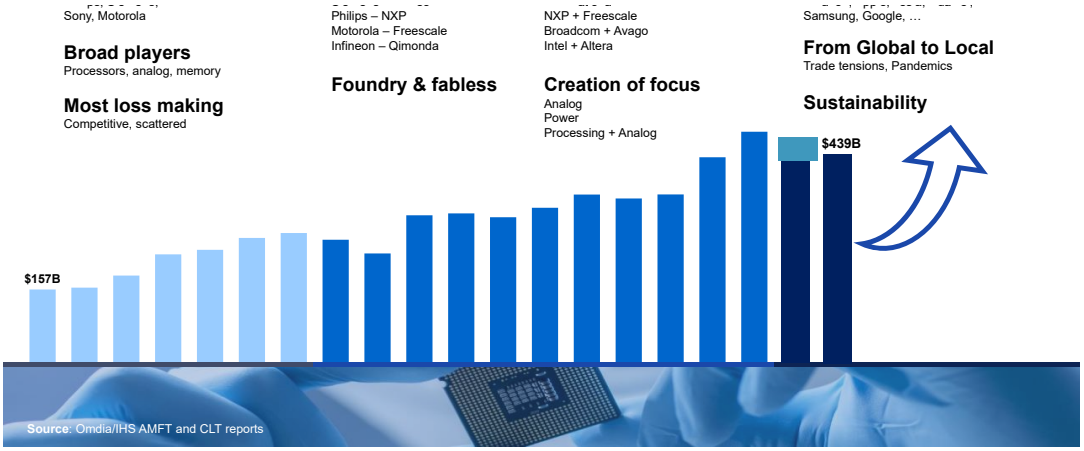
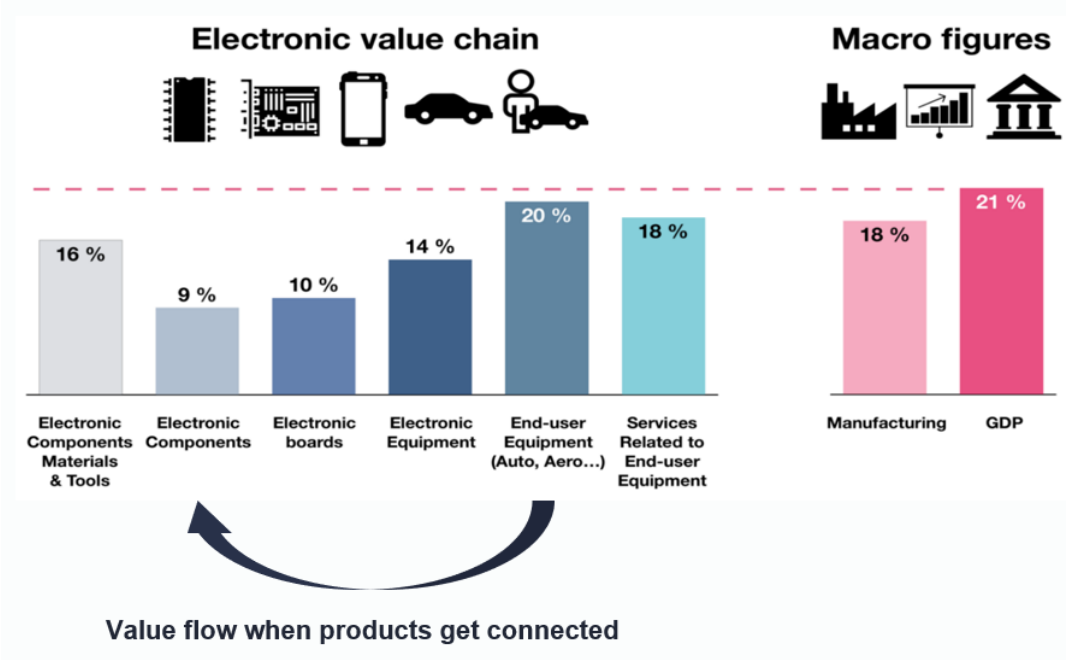


Source: Omdia/IHS AMFT and CLT reports



Source: DECISION études & conseil

The main powerhouse for future connectivity will likely be software applications and the associated ecosystems, much like for mobile handsets over the past decade. It will be largely similar for the enabling technologies. Whoever controls the (de-facto) standards, architecture, and interface specifications will indirectly control the software ecosystem as well. None of today's major software and developer ecosystems for future connectivity are of European origin and there are no signs of change in the near future. . Leading microelectronic businesses in Europe have no significant impact on the global software ecosystem. The only hardware players that can rightfully claim to have any impact are global giants such as Qualcomm, Nvidia, Intel, and ARM who invest heavily in software development. To participate in the market, all others are simply forced to comply with rules and requirements defined by those controlling the ecosystem. Consequently, it is unlikely that the European microelectronics industry will be able to drive any disruptive or truly differentiating innovation beyond its existing position at the bottom of the value chain in future connectivity.

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This reality will not only hamper the communications industry in Europe, but more importantly, affect the European competitiveness and growth across multiple domains. Europe will relentlessly fall further behind the dominating 5G ecosystems today (US and far East) and lose the race towards 6G before it has even started. Unless Europe breaks this trend and proactively establishes investments to enable future connectivity leadership, the European share of the global GDP will be challenged. Action needs to be taken!!

Upon the background of strong demand for semiconductors, and taking into account the recent disruptions of the supply chain, European chipmakers are implementing investment plans in Europe showing a significant increase vs. the previous years. For example, the CEO of STMicroelectronics announced in November 2021 that ST intended to double its production capacity in Europe by 2025[1]. Likewise, Infineon opened in September 2017 a 1.6 billion euro 300 mm plant in Austria, boosting its ability to supply power chips for cars, data centers and renewable power[2], and it announced that it would invest around 2.4 billion euros in 2022, up from about 1.6 billion euros this year, initially investing in existing plants, while not excluding to add more capacity later on[3]. Finally, large production investment was done by NXP at its manufacturing site in Nijmegen in The Netherlands, which has very specialized technologies and focuses on flexible fast customizable manufacturing. No new manufacturing plans are being set up by NXP because of the "asset-light" strategy of the company, in which NXP prefers to have a solid mix of internal versus outsourcing for manufacturing.

When looking deeper into it, these increases in capacity are, for the most part, targeting differentiated technologies where European chipmakers have strongholds, and addressing mainly the markets where they are leaders. For example, in the article mentioned above, Jean-Marc Chery from ST discussed a new business model to be developed jointly with automakers, and stressed the potential of differentiated innovation based on new materials and component architectures, as opposed to being based on miniaturization, citing power devices, image sensors, accelerometers, and microcontrollers. On the other hand, ST intends to address the market for connected objects in a selective way, when it thinks it can bring innovation thanks to those differentiated technologies, like for example for facial recognition on smartphones. Similarly, in a 2020 interview[4], Kurt Sievers, NXP CEO, mentioned that the company had two large segments—automotive and industrial—and a few very well-defined focused plays. It also stressed the company capabilities to address the needs of edge applications. In summary, different European semiconductor stakeholders largely have a common vision in mind, that system designs and specialized technologies are key differentiating and strategic important elements to successfully grow the European semiconductor landscape.

Note: The COREnect roadmap is composed of three documents. Deliverable 3.6 "Final COREnect Industry Roadmap" is the main document, describing the proposed roadmap and providing a summary of all recommendations. Deliverables 3.7 "Core Technologies Development Recommendations and Guidelines" and 2.2 "Consolidated vision and requirement report" are

[1] https://region-aura.latribune.fr/strategie/industrie/2021-11-05/stmicroelectronics-va-doubler-ses-moyens-de-production-en-europe-d-ici-2025-jean-marc-chery-p-dg-895703.html

[2] https://www.reuters.com/technology/infineon-opens-austrian-power-chip-plant-ahead-schedule-2021-09-17/

[3] https://www.reuters.com/technology/chipmaker-infineon-plans-50-investment-boost-2021-10-05/

[4] https://www.mckinsey.com/industries/semiconductors/our-insights/navigating-through-change-an-interview-with-nxp-semiconductors-kurt-sievers

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companion documents to the roadmap. D3.7 provides a synthesis of the industry roadmap and a list of recommendations, guidelines and action proposals, while D2.2 focuses on the investments required to build a stronger European sovereignty in microelectronics and connectivity.

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2 Major developments needed in communication and micro-electronics industry in Europe

The long-term success of European digital industry will depend on how Europe can secure its presence in the overall 5G value chain, i.e., on EU's capability to capture its strengths on digital infrastructure and industry verticals, catalyse research, innovate in the microelectronics domain, and eventually build a full strategic value chain. This shall serve as a solid industry base for attaining European open digital autonomy. This however does not mean necessarily to control all elements of the entire value chain, but rather to focus on controlling essential parts of it, by mastering advanced and competitive technologies, and meanwhile ensure mutual dependencies between different regions. Such a strategy would coincide better and be more secure with respect to global free trade, that benefits Europe and other continents, and at the same time position Europe well, while facing global industry and political challenges. There should be different sources in the supply chain in each technology area, to minimize dependencies, and to maintain alternatives in the supply chain.

To achieve such a strategic goal in the next 10 years, COREnect recommends focusing on the following:

- Secure Europe's leading role in digital infrastructure in terms of demand and supply.
    - Use digital infrastructure such as 5G/6G as a general-purpose innovation and business platform to improve Europe's position in services and applications.
    - Accelerate digital adoption among industries, public administrations, and citizens, to enhance European market drivers.
    - Apply strategical R&I investments to strengthen Europe's capability to supply technologies targeting both infrastructure and devices.
- Establish coordinated R&I funding programmes to support a value chain strategy.
- Employ complementary actions at regulatory level in terms of education, early-stage investments, IPR, and other policy-oriented issues such as public procurement.

2.1 How can we handle the gaps and hurdles (discrepancies) and how can we expand the European eco-system in this domain ?

As outlined in the published COREnect whitepaper[5] in November 2021, Europe is falling behind the US and Asia in the race towards 5G. The availability of broadband internet access is not sufficient in parts of Europe, especially in less densely populated areas or specific regions[6]. In addition to infrastructure, Europe should also strengthen its capability on end-user devices. While it might be difficult to regain a leading position on the mobile handset market, all kinds of novel devices and consumer goods are expected to be connected with 5G/6G, including

[5] https://rebrand.ly/COREnect_white_paper_EU_role_microelectronics

[6] European Commission, Directorate-General for Communications Networks, Content and Technology, Broadband coverage in Europe 2019 : mapping progress towards the coverage objectives of the Digital Agenda : final report, European Commission, 2020, https://data.europa.eu/doi/10.2759/375483

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industrial applications, providing opportunities for European players who are already strong on those markets, as well as for innovative SME's. The impact of cloud/IaaS/SaaS providers on the value chain must also be addressed. To support the growth of their service business, players like Google, Apple, Meta, and Amazon have moved to vertical integration, including designing customized chips to meet their needs (Apple MX, Amazon Graviton2, Google TPU). Unfortunately, Europe does not have any top tier Cloud/IaaS players. This may limit the addressable market of European semiconductor suppliers and in turn Europe's capability to spearhead connectivity and cloud technologies. Consequently, the European Cloud/IaaS ecosystem needs to be supported to secure European sovereignty and leadership.

In the COREnect project, different actions have already been proposed to handle the identified gaps to reach the long term wanted position for Europe. These include the need to actively establish both vertical and horizontal industry alliances to create European leadership for both digitalization of applications and the enabling technologies. Europe must support funding programmes to allow such alliances, thus building up knowledge, know-how, and IPRs for all elements in the value chain. Coordinated public and private actions are needed with a multi-year time perspective in line with current instruments, e.g. Horizon Europe, Smart Networks & Services, EUREKA clusters, IPCEI programs, the newly announced European Chips Act etc. In addition to these strategic large-scale and long-term funding schemes. Europe could further explore the possibility to provide flexible and fast-track options, with potentially lower funding amounts to stakeholders from industry, RTO, and academia, in the chipset value chain. A 6G component platform could also be created as well as pan-European sandboxes, where SMEs would automatically be eligible to offer products and services throughout the EU market.

When it comes to SMEs, there is a trend in the 5G/6G ecosystem to primarily position SMEs as technology users, rather than technology providers -and as more interested in short-term results. Analysis of SME participation in the 5G PPP however cannot demonstrate whether this is an actual tendency or not. In the ECS ecosystem, The Chips Act, as well as the Member States' "European initiative on processors and semiconductor technologies" also seem to primarily position SMEs as technology users, except for those "active in the design front". Here as well, participation in ECS research projects (ECSEL, PENTA, CATRENE…) show that SMEs are also technology providers.

Therefore, SMEs shall be considered as potential contributors and stakeholders both in the technology and in the (vertical) applications ecosystems. This means that it is important to invest both in microelectronics and connectivity technology as well as vertical sectors using those technologies, as far as SMEs are concerned.

COREnect has also addressed a need to reform the European regulatory framework. Like other ecosystems (primarily China and the US) Europe must increase flexibility for state-aided initiatives and favourable conditions for R&D investments. Potential means to be considered include:

- Flexible and streamlined applications for state aid programs.
- Tax benefits for R&D investments on identified critical technologies.
- Incentives to invest and drive global standardization activities.
- Incentives for deploying and using leading digital technologies.
- Financial instruments to support company acquisitions within Europe in strategically important areas.

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- Easier real estate and property handling for emerging and fast-growing businesses.
- Investments in education to secure leading skills in cutting edge technologies.
- Public procurement policies to favour a European open digital autonomy.

Both Member States and the EU Commission must ensure a level playing field for global actors, and agree on a common European trade strategy. There should be a careful balance between open global trade and securing European interests to secure strategic know-how and support companies while remaining transparent and open towards business partners.

Building the most relevant European ecosystems in microelectronics and connectivity could be done through a series of supporting measures such as:

- Strengthen the interaction between corporate companies, research organisations, and SMEs. The main objective is to gather the best researchers in the field and ensure that Europe will be at the edge of components for 6G.
- Enable matchmaking between European SMEs, and with other European stakeholders. This should cover technology, innovation, education, finance, and funding. It shall be oriented not only towards start-ups, but also towards spin-offs and established SMEs. The main objective is to overcome the issue of Europe not succeeding in creating companies worth hundreds of billions of euros (like what is being achieved in the US and China).

In other words: help create a European community / ecosystem combining microelectronics and connectivity, able to compete at global level. This may well lead to creating one or more European champion(s) in the field, who could then “lead the way” for Europe.

2.2 COREnect-based priorities in European Research & Innovation Roadmaps/Agendas

The COREnect deliverable D3.4 “Intermediate COREnect industry roadmap” contains key recommendations/actions provided by the three expert groups created to cover COREnect strategic focus areas: (1) compute and store, (2) connect and communicate, and (3) sense and power, and address four market segments: (1) connectivity infrastructure, (2) consumer grade connectivity, (3) industrial grade connectivity, and (4) automotive connectivity.
Those recommendations and actions are diverse in nature, and span from research to standardisation activities, through skill development and infrastructure programs. In this sub-section, we consider only the recommendations pertaining to research and innovation.

2.2.1 Topics related to micro-electronics

Among those, the main topics related to electronics components and systems and emerging from the work of the COREnect expert groups are listed below:

- Further develop new technologies for embedded non-volatile memories (eNVM), which are of high interest not only because of their low energy consumption and high speed, but also as an enabler for local data processing at the edge and subsequent network workload decrease;

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- Develop devices capable of operating at 300 GHz and beyond frequencies, investigating many materials: FDSOI, SiGe, BiCMOS, but also III-V devices (especially InP and GaN), for which integration with silicon must also be developed;
- Thermally efficient packaging technologies for wireless circuits with frequencies ranging from millimeter waves to THz;
- Testing of millimeter-wave and THz circuits;
- Integrated photonics technologies (silicon photonics, III-V-based photonic ICs);
- Developing digital devices and components capable to operate with baud rates far beyond 100 Gbauds, to enable the full benefit of optical transmission;
- Heterogeneous integration: this covers many technologies, from 2.5D and 3D chip- and wafer-level integration, including chiplets, to embedded passive or active components in substrates, up to System-in-Package, and technologies required for co-package electronics and optical interfaces;
- Developing AI cores for edge processing;
- Research on Si batteries, integrated batteries, energy harvesting technologies, micro solar panels;
- Integrated THz imaging;
- Joint communication and sensing (in particular with radar chipset architectures which could combine sensing and communications);
- Although there is no specific call for research on (cyber)security and authentication technologies in the COREnect deliverable D3.4, the need to implement those technologies to ensure trusted end-to-end communications is often mentioned.

2.2.2 Intersection points with the ECS SRIA

It is interesting to see to what extent those priorities are reflected in the 2022 Electronic Components and Systems Strategic Research and Innovation Agenda (ECS SRIA for short), which was published on January 2022, results from the collective work of over 300 experts across the whole value chain of the domain beyond connectivity. Its structure is represented by the following picture.

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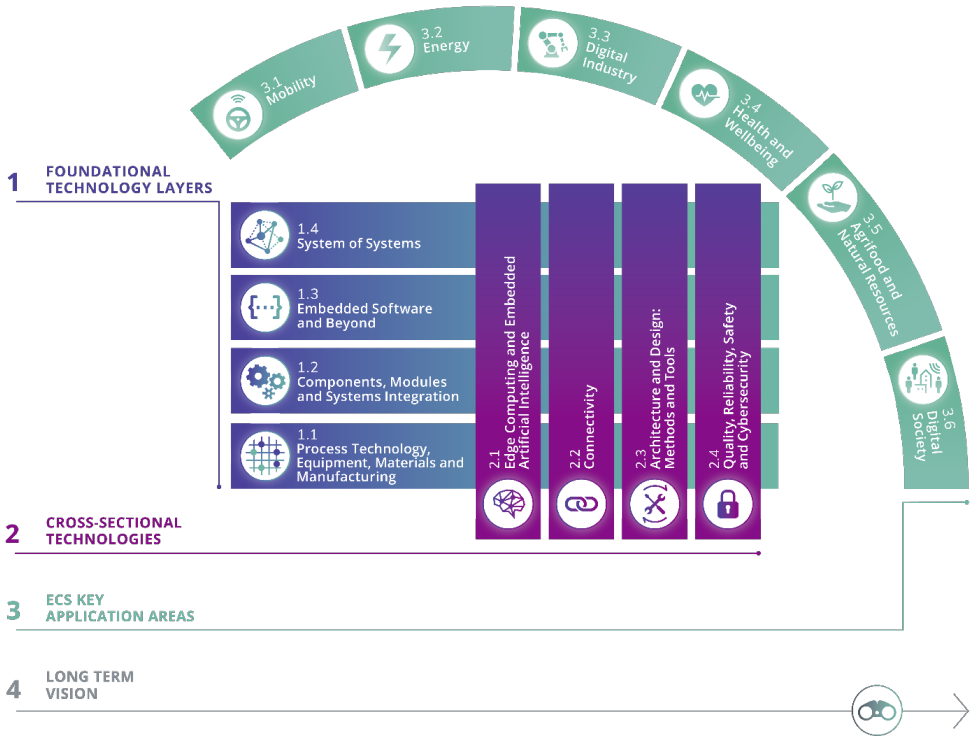

Source: AENEAS, ARTEMIS-IA and EPOSS

The first part of the ECS-SRIA is composed of four chapters focused on the **Foundational Technology Layers** and their technical challenges along the technology stack, from materials and process technology to components, modules and their integration into electronic systems, embedded software developments and software technologies, to full systems and Systems of Systems. These foundational are complemented by four **Cross-Sectional Technology** chapters that focus on transversal areas of scientific research and engineering, where innovative results emerge from the joint contribution of the foundational layers to those specific areas. In the third part of the ECS-SRIA, six **Application** chapters describe the challenges arising from specific ECS application domains that are key for Europe and identify the R&D&I efforts required by these application domains as regards ECS. Finally, the **Long-Term** seeks to identify the research subjects that must be addressed at low TRL levels as foundation and preparation for the crucial developments in European industry over the next decade.

The ECS SRIA has therefore a wider scope than the one addressed by the expert groups of the COREnect project. On the other hand, it is specifically containing Research and Innovation actions, while the COREnect expert groups have also listed non-R&I items such as policy- or industry-level activities (regulation, standardization, etc…). The question is therefore whether R&I actions identified by the COREnect expert groups are indeed covered in the ECS SRIA.

To a great extent, the answer is positive. As can be inferred by the ECS SRIA structure, the SRIA "connectivity" chapter is echoing many priorities listed by the COREnect experts:

The Major Challenge 1 identified in that chapter advocates strengthening the EU connectivity technology portfolio to maintain leadership, secure sovereignty and offer an independent supply chain. It translates in the more detailed actions listed below:

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- Innovative differentiated semiconductor technology development targeting connectivity applications, including advanced BiCMOS, RF SOI, GaN, FD SOI and GaAs/InP;
- Innovative packaging and PCB technology targeting connectivity application;
- Innovative semiconductor equipment enablement;
- Innovative connectivity solution development targeting hardware, IP and software virtualization;
- Heterogeneous integration (multi-die system in a package, advanced assembly capability, advanced substrate manufacturing, etc);
- Ultra-low power transceivers;
- Antenna and packages at mm-wave and THz, on-chip antennas;
- Meta-materials for antennas, meta-materials for intelligent reflective surfaces and meta-surfaces

In addition, the Major Challenge 2 calls for investigation of innovative connectivity technology (new spectrum or medium) and new approaches to improving existing connectivity technology to maintain the EU's long term leadership. In particular, it mentions that special focus should be dedicated to the frequency bands listed below:

- SubTHz connectivity application in the 200 GHz – 300 GHz band
- Encourage European activity in the spectrum > 300 GHz to play a role in the development of the new technology and assess its relevance to future 6G standards.
- Investigation and standardisation activity targeting 6G cellular application in the frequency band < 10 GHz.
- development of innovative connectivity technology using unlicensed frequency in the 6 GHz – 7 GHz band.

That Major Challenge also mentions other research axis such as

- development of innovative connectivity system using new propagation mediums.
- development of connectivity system leveraging the concept of edge AI.
- evaluation of the AI concept to handle the complexity of future connectivity networks (for example, 6G), and to improve efficiency and adaptability.

In addition, COREnect priorities related to materials, device and packaging technologies are developed in two SRIA foundational technology chapters:

- Chapter "Process Technology, Equipment, Materials and Manufacturing"
- Chapter "Components, Modules and Systems Integration"

More details on the different topics covered in these two chapters can be found in Annex (Section 6.1).

The need for trusted end-to-end communications also has an impact on the research agenda to be addressed by the ECS community. Here, details are mostly provided by the ECS SRIA in its Chapter "Quality, Reliability, Safety and Cybersecurity", and more precisely by its Major Challenge 3, "Ensuring cyber-security and privacy"

To complete that overview of communications-related topics of the ECS SRIA, we can mention that its Long Term Vision chapter identifies further research needs on III-V MOSFET devices (including 3D processing aspects) for millimeter-wave front-ends, alternative memories, beyond-von Neumann architectures, silicon photonics, and closer integration of electronics and

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photonics with PICs and fast semiconductor driving/control/sensor components. This again largely echoes the research priorities listed by the COREnect Expert Groups.

There are, however, a few topics identified by those experts which are currently not or only very lightly touched upon by the ECS SRIA, most notably:

- Testing of millimeter-wave and THz circuits;
- Developing digital devices and components capable to operate with baud rates far beyond 100 Gbits, to enable the full benefit of optical transmission;
- Joint communication and sensing (in particular with radar chipset architectures which could combine sensing and communications).

It would probably be beneficial for the ECS and SNS experts to further discuss the expectations and needs on these topics.

Finally, a few other R&I topics identified as needed by the COREnect experts are so far considered outside of the scope of the ECS community, such as:

- Open modular microkernel-based Operating Systems;
- Research on power transmission over fiber

2.2.3 Topics related to telecommunication systems

Performing the same exercise of analyzing the COREnect deliverable D3.4 “Intermediate COREnect industry roadmap” for telecommunication systems a similar list of topics can be extracted. Note that the following topics have been identified from both the analysis of the research area as well as related recommendations:

Technological Areas:

- Significant increase in data rate, traffic capacity, connectivity density, network latency, coverage, energy efficiency, spectrum efficiency
- Evolved RAN to address multiple standards, meeting extreme low latency constraints and supporting new cell-free and software-based radio systems
- Increased RAN computing capability – virtualized RAN
- Advanced MIMO and uMIMO signal processing, support of beamforming, including distributed (coordinated) beamforming by multiple IoT devices
- mm-wave beamforming transceiver and front-end design
- Ultra-dense deployment of access points
- New materials for active devices
- Optoelectronic based mm-wave and sub-THz generation and processing by heterogeneous integration with photonics technologies (silicon photonics and III-V-based)
- Work on integration approaches for photonics and electronics that allow a dense integration of a large amount of programmable accelerators for real-time, latency specialized and hardware-based AI solutions
- Analog radio-over-fiber or hybrid communications solutions
- Joint communication and sensing
- Adaptive resource management, meeting power and thermal constraints
- Develop solutions for Time-Sensitive Networking

Related Recommendations

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- Deploy 5G & 6G in EU as thoroughly as possible
- Collect and organize access to Europe-specific datasets for AI training with components that have privacy
- Foster digitization of European industries
- Launch EU funded collaborative RIA projects on telecom applications operating in the W-band (75-110 GHz) and D-band
- Define 5G/6G system requirements for semiconductor components and participate in 5G/6G standardization.
- Build demo systems based on OpenRAN, campus networks, and vehicle-to-X communications;
- Continuous investing in heterogeneous integration technology R&D
- Keep up to date with and validate (private) 5G URLLC systems (trials, testbeds)
- Launch EU funded collaborative RIA projects targeting industry grade communication systems and solutions, stimulating cross-disciplinarity
- Define a consistent EU spectrum policy, considering licensed and unlicensed and global and local licenses
- Develop prototypes of industry grade connectivity using 6G innovations
- Create an edge Computing Strategy, which is suitable to use technologies available in Europe
- Work on further regulation, standardization, authentication forV2V, V2X communication e.g., C-ITS (collaborative, intelligent, transportation System
- Develop and deploy a modular secure OS framework, European cloud, and hypervisor technology
- Ensure secure and privacy-respecting local storage
- Native AI support in multiple domains/devices
- Invest in high-frequency, thermally efficient packaging substrate technologies with embedded antenna array elements.

2.2.4 Intersection points with the Smart Networks and Services SRIA

It is interesting to see to what extent those priorities are reflected in the Smart Networks and Services SRIA (SNS SRIA for short[7]), which was published on December 2021. The SNS SRIA has been developed from the collaboration of the 6G Smart Networks and Services Industry Association (6G-IA) and the NetworldEurope European Technology Platform (ETP). These organizations, together with the supporting associations are representing more than 1000 entities, involved in the 5 % of European GDP, and are contributing to the definition of research areas especially in the domain of communication systems and networks. NetWorldEurope has formed a detailed SRIA[8] for 2021-2027. The 6G-IA has taken the NetworldEurope's SRIA into consideration and used it as the basis for the SNS SRIA. Since 28.04.21 the two organizations

[7] https://ec.europa.eu/newsroom/dae/redirection/document/82079
[8] NetworldEurope, Smart Networks in the context of NGI, 2020: https://bscw.5g-ppp.eu/pub/bscw.cgi/d367342/Networld2020%20SRIA%202020%20Final%20Version%202.2%20.pdf

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have setup a collaboration framework[9] that defines exactly this process for the preparation and adoption of the SNS SRIA.

In relation to the produced recommendation from COREnect D3.4 and as captured in the previous subsection, one can notice that these have been also present as objectives in the key SNS objective since the time the SNS Partnership was a proposal[10]. More specifically SNS objectives include:

- ensuring EU competitive edge and sovereignty of the EU industry through a value chain approach covering EU technological capabilities in devices (IoT), networks and service platforms (edge computing);
- Supporting large scale digitisation of EU industry through SNS platforms covering the most demanding use cases;
- Supporting the emergence of new classes of applications, opening new economic opportunities;
- Addressing societal needs, notably as outlined in the Green Deal and SDG's;
- Supporting European access and inclusion to new high skilled jobs;
- Promoting Europe as a lead market for specific use cases (focus on automotive to leverage CEF2 activities).

The NetworldEurope SRIA has been used as the basis for the development of the SNS Partnership SRIA. It must be noted at this point that the NetworldEurope SRIA contains a superset of topics, some of which do not fall directly into the scope of the SNS Partnership, but rather in other HEU related Partnerships (e.g., KDT, Photonics21, etc.). Thus, a specific methodology has been developed, involving members of the 6G-IA as well as other Associations supporting the SNS Partnership (i.e., AIOTI, CISPE.cloud and NESSI).

The list of selected topics, as selected by experts and fine-tuned through consultations have been organized in 4 Streams. More specifically,

- **Stream A:** Targets the development of smart communication components, systems, and networks following the further evolution of 5G systems. It follows an evolutionary path towards the development of 6G networks, relying on the development of an intermediate technology point. The proposed research topics are complementary and altogether support a complete system view.
- **Stream B:** Covers research for revolutionary technology advancements, in preparation for 6G and revolutionary advancements of IoT, devices and software. This Stream targets Low Technology Readiness Level (TRL) technologies that are expected to deliver innovative solutions towards real life networks in a long-term time-period.
- **Stream C:** Focuses on SNS Enablers and Proof of Concepts (PoCs) used to develop experimental infrastructure(s), ideally aiming to be used during later phases of the SNS.
- **Stream D:** Targets towards large-scale SNS Trials and Pilots with Verticals, including the required infrastructure. The aim is to explore and demonstrate technologies and advanced applications and services in the vertical domains. Phase 1 Stream D projects

[9] 5G-IA & NetworldEurope ETP joint press release: https://5g-ppp.eu/the-5g-ia-and-networldeurope-etp-sign-collaboration-agreement/

[10] Smart Networks and Services proposal, 30.06.2020: https://ec.europa.eu/info/sites/info/files/research_and_innovation/funding/documents/ec_rtd_he-partnership_smart-networks-services.pdf

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should incorporate as possible technologies that currently appear as key enablers for 6G networks, e.g., AI/ML, cybersecurity, high performance computing, advanced IoT solutions, etc. During the subsequent SNS phases, Stream D infrastructures will mostly rely on SNS phase 1 technologies and especially the infrastructures to be developed from Stream C projects. The goal is to gradually incorporate innovative 6G functionalities.

The challenge in stream A is to develop the technologies supporting mid-term functional and non-functional properties. It also requires realising seamless and cost-effective integration of multiple enablers from related domains (e.g., HPC, (cyber-)security, AI/ML, IoT) with the objective to prepare strong European industrial positions for the further mid-term evolution of 5G standards expected in upcoming 3GPP Releases and eventually moving towards the 6G era.

The topics of Stream A include:

- Green radio technology: address basic building blocks that go beyond current 5G specifications (e.g., PHY layer topics, hardware acceleration, cell-free, software-based radio, improvements on mmWave, BC/MC architectures, EMF impact, considering enablers such AI/ML, to minimize energy consumption)
- Ubiquitous radio access: Impact on coverage, accelerate the deployment, integrated terrestrial and non-terrestrial components, highly consolidated NTN architectures
- Sustainable capacity networks: focus on transport networks, converged packet-optical transport network, improve network capacity, increased programmability, control latency taking into consideration energy consumption.
- Towards Smart Green Systems: develop architectures to jointly optimize the energy consumption of all elements of the future SNS systems. Improving SBA solutions, use enablers e.g., Artificial Intelligence for programmable and energy optimized cloud and edge computing solutions.
- Evolution on Cloud/Edge Computing architectures and operational support: open, distributed, virtualized and possibly decentralised, edge computing architectures and implementations. Consideration of new IoT device management techniques will appear, expecting to operate over distributed architectures for IoT systems. A clear technological strategy for edge integration into a cloud continuum offering opportunities for European cloud/edge technology suppliers and supporting various edge/access integration scenarios, (e.g., NTN). Create a data space to help the planning for operations in distributed and decentralized environments.
- Trustworthy and Reliable End to End connectivity Software platforms : Projects should evolve security of 5G towards the notion of building and maintaining Trust in deployed and interconnected 5G systems and services. The outcome should build trust and reliability, significantly advanced beyond the baseline security measures of 5G.
- Real-time zero-touch service technologies: develop a framework for an effective service deployment and management, zero-touch software strategies pursuing the ambitions of the Green Deal, including open-source technologies operating at optimal energy performance

Stream B consequently targets revolutionary technologies of low TRL (2-4) technology advancement as required for future 6G systems. It takes a holistic research approach towards the needed technology, with a value chain perspective covering an integrated ecosystem with IoT, devices and software-based solutions in unified networks. From a comprehensive system

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perspective, the target is a globally connected continuum platform with the convergence of networks and IT systems to enable new future digital services. This continuum must provide users with improved performance, higher level of control, increased transparency in interactions with digital services, adequate support of ethical values and conformance with societal requirements and readiness (e.g., GPDR, EMF awareness, etc.) whilst contributing to key SDG's. Stream B technological topics are grouped in four strands as follows:

in Strand 1 (System Architecture) the following topics are to be investigated:

- Technologies for scaling Inter-computing systems
- Control and controllability separation
- Frictionless inter-domain resource management
- Native integration of AI for telecommunications
- New Data Transfer Paradigms with deep Edge integration
- Improve data plane performance
- Deterministic Networking

In Strand 2 (Wireless Communication Technology and Signal Processing) the following topics are to be investigated:

- Terahertz Communications and Ultra-Massive MIMO
- Joint communications and sensing
- New Waveforms, Random and Multiple Access
- Enhanced Modulation and Coding
- Wireless Edge Caching
- Human-friendly Radio systems
- Spectrum Re-farming and Reutilisation

In Strand 3 (Communication Infrastructure Technologies and Devices) the following topics are to be investigated:

- Flexible Capacity Scaling
- Ultra-high Energy Efficiency
- Integration of Optical and Wireless Technologies
- NTN Infrastructures
- Integrated NTN service provision
- New IoT components and devices
- Troposphere Networking
- New Physical Layers
- Nano-things networking

Finally, in Strand 4 (Secure Service Development and Smart Security) the following topics are to be investigated:

- Human-centric security and privacy technologies
- Holistic smart service development frameworks
- Secure lifecycle service management and smart operation
- Enhanced service features for fostering security
- Efficient security enablers for dynamic heterogeneous untrusted environments

Stream C and Stream D are dealing with the deployment and use of experimental platforms that will enable the realization (deployment, testing and validation) of several of the recommendations as captured by the COREnect experts. As can be inferred by the SNS SRIA structure, it captures many priorities listed by the COREnect experts.

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More specifically, revisiting the abovementioned list of technological areas as depicted in COREnect's D3.4, these can be indicatively also found in several activities in the SNS research activities:

Technological Areas in D3.4	**Technological activities in SNS SRIA**
Significant increase in data rate, traffic capacity, connectivity density, network latency, coverage, energy efficiency, spectrum efficiency	These topics are present in multiple activities but more prominently in **Stream A**: Green Radio Technology, Ubiquitous Radio Access, Sustainable Capacity Networks, Evolved Architecture of Global Green Systems and in **Stream B**: Wireless Communication and Signal Processing (Terahertz Communications and Ultra-Massive MIMO, New Waveforms, Random and Multiple Access, Enhanced Modulation and Coding, Spectrum Re-farming and Reutilisation) and Communication Infrastructure Technologies and Devices (Flexible Capacity Scaling, Ultra-high Energy Efficiency, New Physical Layers and associated protocols)
Evolved RAN to address multiple standards, meeting extreme low latency constraints and supporting new cell-free and software-based radio systems	These topics are present in multiple activities but more prominently in **Stream A**: Green Radio Technology, Ubiquitous Radio Access and in **Stream B**: Wireless Communication and Signal Processing (Terahertz Communications and Ultra-Massive MIMO, New Waveforms, Random and Multiple Access, Enhanced Modulation and Coding, Human Friendly Radio systems, Spectrum Re-farming and Reutilisation)
Increased RAN computing capability – virtualized RAN	These topics are present in multiple activities but more prominently in **Stream A**: Green Radio Technology, Edge Computing Evolution, **Stream B**: System Architecture (Frictionless inter-domain resource management), **Stream C**
Advanced MIMO and uMIMO signal processing, support of beamforming, including distributed (coordinated) beamforming by multiple IoT devices	These topics are present in multiple activities but more prominently in **Stream A**: Green Radio Technology, Ubiquitous Radio Access and in **Stream B**: Wireless Communication and Signal Processing (Terahertz Communications and Ultra-Massive MIMO, New Waveforms, Human Friendly Radio systems)
mm-wave beamforming transceiver and front-end design	**Stream A**: Green Radio Technology, Ubiquitous Radio Access
Ultra-dense deployment of access points	**Stream B**: Wireless Communication and Signal Processing (Human Friendly Radio Systems)

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New materials for active devices	**Stream B**: Wireless Communication and Signal Processing (Terahertz Communications and Ultra-Massive MIMO)
Optoelectronic based mm-wave and sub-THz generation and processing by heterogeneous integration with photonics technologies (silicon photonics and III-V-based)	**Stream B**: Wireless Communication and Signal Processing(Joint communication and sensing)
Work on integration approaches for photonics and electronics that allow a dense integration of a large amount of programmable accelerators for real-time, latency specialized and hardware-based AI solutions	**Stream B**: Communication Infrastructure Technologies and Devices (Flexible Capacity Scaling, Integration of Optical and Wireless technologies)
Analog radio-over-fiber or hybrid communications solutions	**Stream B**: Communication Infrastructure Technologies and Devices (Ultra-high Energy Efficiency)
Joint communication and sensing	**Stream B**: Wireless Communication and Signal Processing(Joint communication and sensing)
Adaptive resource management, meeting power and thermal constraint	**Stream A**: Evolved Architecture for Global Green Systems, Real-Time Zero-touch Service Technologies, **Stream B**: System Architecture (Technologies for scaling Inter-computing systems, Control and controllability separation, Frictionless inter-domain resource management)
Develop solutions for Time-Sensitive Networking	**Stream B**: System Architecture (Deterministic Networking)

2.3 European Funded Programs on micro-electronics and telecommunications

To make Europe a true champion of digital infrastructure for both supply and demand, it is paramount to develop and foster European ecosystems and value chains with coordinated public and private actions. Europe must support funding programs to allow both vertical and horizontal industry alliances, thus building up knowledge, know-how, and IPRs for all elements in the value chain. This may require multi-year programs with a value chain strategy, using instruments such as: Horizon Europe including Public-Private Partnerships, e.g., Key Digital Technologies (KDT), Smart Networks & Services (SNS), and Connected, Cooperative and Automated Mobility (CCAM); the Digital Europe Program; the Connecting Europe Facility (CEF) including CEF Telecom and CEF Digital; EUREKA Clusters, e.g., Xecs, CELTIC-NEXT, ITEA; Important Projects of Common Interest (IPCEIs); National R&I programs. In addition to long-term and large-scale funding pro- grammes, Europe could further explore the possibility to provide flexible and fast-track options, with potentially lower funding amounts to stakeholders from industry, RTO, and academia, in the chipset value chain. As demonstrated by the COVID-

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19 emergency research program, such small or mid-scale flexible programs would help the timely formation of research alliance and development in R&I areas where urgent actions are required. Cooperation between companies, research organisations, and SMEs, must be promoted. R&I programs should enable matchmaking between European SMEs and other stakeholders, covering not only technology and verticals, but also innovation, education, finance, and funding. Strengthening the interaction between SMEs and other players in the telecom and the ECS do- mains, as well as with vertical stakeholders, shall be a priority. In general, there should be a clearer link between the overall European industrial strategy towards a sustain- able technological sovereignty and activities supported by R&I funding programs.

2021 has been a year of profound renewal for the various public funding instruments supporting research and innovation across Europe. It witnessed the start of Horizon Europe, the most ambitious EU Research and Innovation program ever, as well as the adoption of the Single Basic Act and the publication in the Official Journal of the Council Regulation (EU) 2021/2085, establishing ten European Joint Undertakings (JUs), including the Key Digital Technologies (KDT)[11] and the Smart Network and Services (SNS)[12] Joint Undertakings. Complementary to Horizon Europe, the European Commission launched the Digital Europe Program (DIGITAL), which is a new EU funding program focused on bringing digital technology to businesses, citizens and public administrations and providing strategic funding in five key capacity areas: supercomputing, artificial intelligence, cybersecurity, advanced digital skills, and the wide use of digital technologies across the economy and society. 2021 also saw the start of the new Eureka Clusters Program (ECP), with Xecs addressing the Electronics Components & Systems (ECS) community, and Celtic-Next investigating next-generation communications.

Over the period 2021-2027, KDT shall receive up to €1.8 billion from the EU, a steep increase over the €1.2 billion for ECSEL. Matching investments i.e., up to €1.8 billion shall come from participating states. The total R&I project volume should reach more than €7 billion. In relation to the SNS JU, the overall funding shall be €900 million from the EU with at least equal funds being matched by the private sector over the period 2021-2027.

It is harder to estimate the amount of funding available within the Eureka Clusters Programme. For example, while some countries (Germany, The Netherlands) have indicated that they provide up to 10 M€/year each over the period 2022-2025 for the Xecs Cluster, many other countries operate with an open budget, which means that funding will change from call to call depending on the proposals received and labelled. Nevertheless, expecting potential total public funding for Xecs in the range of 45 to 55 Mio € per year is probably not too far off the mark.In addition, many countries have identified ECS and/or SNS as strategic fields to be supported for their economic and societal benefits, and have put in place national funding programs to foster R&I projects in those domains.

Overall, the funding landscape for European R&I in the ECS and SNS domains can therefore be represented in the picture below.

[11] https://www.kdt-ju.europa.eu/ In the near future the KDT JU shall become the “Chips JU”, as announced in the “Chips Act”.

[12] https://digital-strategy.ec.europa.eu/en/policies/smart-networks-and-services-joint-undertaking

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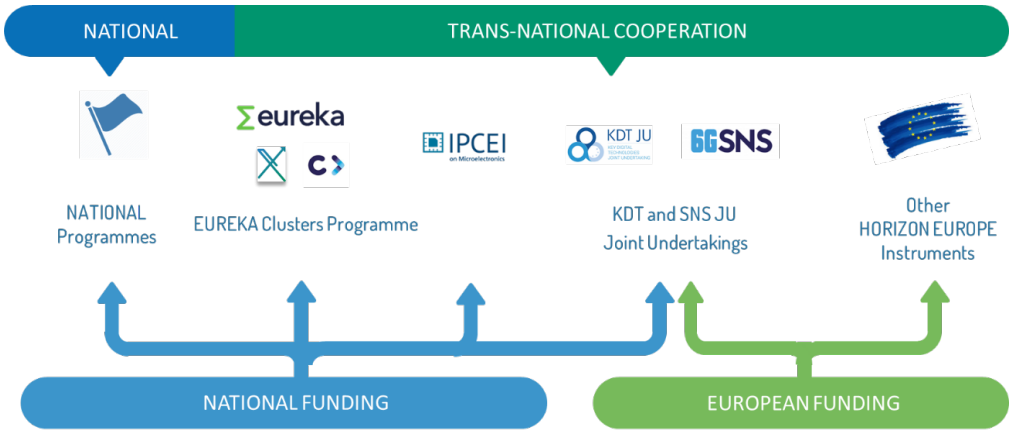

Source: AENEAS

The Strategic Research and Innovation Agendas generated by the ECS, SNS and CELTIC-NEXT communities are the main basis for the programs being part of the European landscape: The KDT workplan is elaborated from the ECS SRIA contents, and the Xecs Cluster, which is the Eureka Cluster supporting the ECS value chain within the ECP, explicitly acknowledges the ECS SRIA as describing its technical scope. As was discussed in section 2.2 of the current document, R&I actions identified by the COREnect expert groups are to a great extent covered in the ECS SRIA, and therefore are supported both within the KDT JU and the Eureka Clusters Program.

Likewise, as mentioned in section 2.2. for SNS JU, the NetworldEurope has formed a detailed SRIA about the smart networks and services in the context of Next Generation Internet. The 6G-IA in cooperation with DG-CNECT have taken the NetworldEurope's SRIA into consideration and used it as the basis for producing the SNS SRIA[13]. From the SNS SRIA, the most suitable topics have been selected and included in the first SNS R&I Work Programme (WP). As presented in section 2.2., the SNS WP contains the R&I topics and actions as identified by the COREnect expert groups.

Another mechanism of interest to support the priorities identified in the COREnect project is the Important Project of Common European Interest (IPCEI). In fact, IPCEI is not a funding program per se, but a revised state-aid framework. Contrary to usual state-aid regulations, it allows Member States to extend their financial support beyond purely Research and Innovation activities and include as well first-time industrialisation, i.e. covering the inefficient part of an investment project, which pure market mechanisms would not be able to justify. As a counterpart, there is a quite rigorous state-aid notification process.

As the name indicates, activities benefiting from that framework must make a substantial difference, address specific interest of Europe and display essential spill-over effects visible across the continent.

On December 20th, 2021, Germany – on behalf of the participating Member States – formally pre-notified to the Commission the new IPCEI on Microelectronics and Communication Technologies. This IPCEI is driven by the needs of European industry for trustworthy microelectronics components and systems incl. hard- and software, and for communication systems. Its strategic goals are the following:

[13] https://digital-strategy.ec.europa.eu/en/policies/sns-governance

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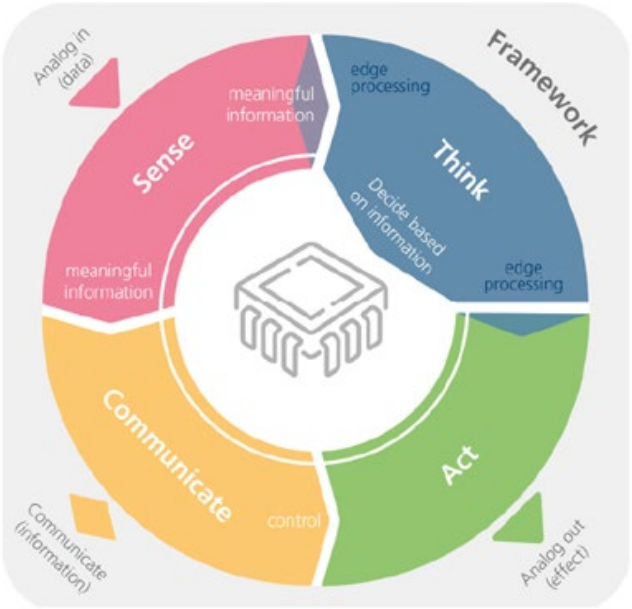
- Creating microelectronics and connectivity solutions beyond global state-of-the-art which enable the digital transformation.
- Pushing for the most energy-efficient and resource-saving electronics systems and manufacturing infrastructure.
- Establishing, ensuring and driving European standards in data and cyber security on every level of the microelectronics value chain, especially in the communications domain.
- Countering market failures in and reinforcing susceptible sections of the European microelectronics and communication technologies value chains.
- Significantly increasing the manufacturing of innovative microelectronic products in Europe

These strategic goals clearly echo the concerns which gave rise to the COREnect project, and one can expect that COREnect-identified priorities will be fully supported by that project.

The IPCEI is comprised of 4 workstreams, responding to the complementary objectives along the microelectronics value chain.

- Think addresses processors and memory as the brain of a computer.
- Sense addresses the organs of perceptions which generate the data to be processed.
- Act addresses the body and muscles of an electronic system.
- Communicate addresses the strong nerve pathways which network with the brain.



Source VDI/VDE-IT

Each work-stream is further structured into four work packages: Tools and technologies, Semiconductor technologies, Components and Modules, and Subsystems and Systems, which closely reflect the foundational technology stack of the ECS SRIA.

The status of the IPCEI ME/CT as of February 1st, 2022, evidences its very significant size and potential impact:

- 17 Member States have started prenotification at the European Commission in December 2021
- Member States are involved with associated participants, which do not need notification

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- 2 Member States are prospective Member States
- 112 Direct participants (Large enterprises, SMEs, Start-ups) covering the entire value chain of microelectronics
- 32 Associated participants (Large enterprises, SME, Research Organisations)

In addition to the initiatives mentioned above, there are a few EU-level instruments designed to specifically support SMEs, including in the domains of microelectronics and connectivity. Although those instruments focus primarily on trying to bridge the gap between R&I and market take-up, there is funding dedicated to promoting breakthrough innovation, especially via the Eurostars program dedicated to innovative SMEs, and the European Innovation Council and its top-down calls in the digital domain[14].

Finally, the European Commission's proposal for a European Chips Act (the "Chips Act") aims to more than double Europe's share in global semiconductor production capacity to 20% by 2030. This objective appears very ambitious as Europe has fallen behind in semiconductor manufacturing, declining from 24% of global production capacity in 2000 to 8% today. Although not an R&I programme on its own, it shall serve as a framework for strengthening microelectronics and connectivity within R&I initiatives all over Europe.

2.4 Positioning of Europe versus the US and China

Over the next ten years, the industry will need to invest about $3 trillion in R&D and capital expenditure in order to meet the increasing demand for semiconductors. Global stakeholders (industry, governments, etc.) must collaborate to continue facilitating worldwide access to markets, technologies, capital, and talent, and make the supply chain more resilient.

While worldwide distribution of supply chain and geographic specialization had a positive impact on European consumer, it has created dependencies and vulnerabilities. Manufacturing emerges as a major focal point when it comes to the resilience of the global semiconductor supply chain. About 75% of semiconductor manufacturing capacity, as well as many suppliers of key materials—such as silicon wafers, photoresist, and other specialty chemicals—are concentrated in China and East Asia. Europe has historically contributed to the emergence of semiconductor industry but accounts today of ≤ 20% across the global semiconductor supply chain (see figure below). However, Europe still have leading edge IDM semiconductor industrial suppliers (Infineon, NXP, STm), a dominant position in Extreme UV lithography equipment (ASML) that are used to manufacture advanced CMOS node chips and several leading semiconductor research institutions (CEA-Leti, Fraunhofer, IMEC,…).

A - The global semiconductor supply chain based on geographic specialization has delivered enormous value for the industry

[14] "One of the SNS Program KPIs is the participation of SMEs at the RIA and IA activities at a level of 20%", SNS R&I Work Program 2021-2022, Smart Networks and Services Joint Undertaking.

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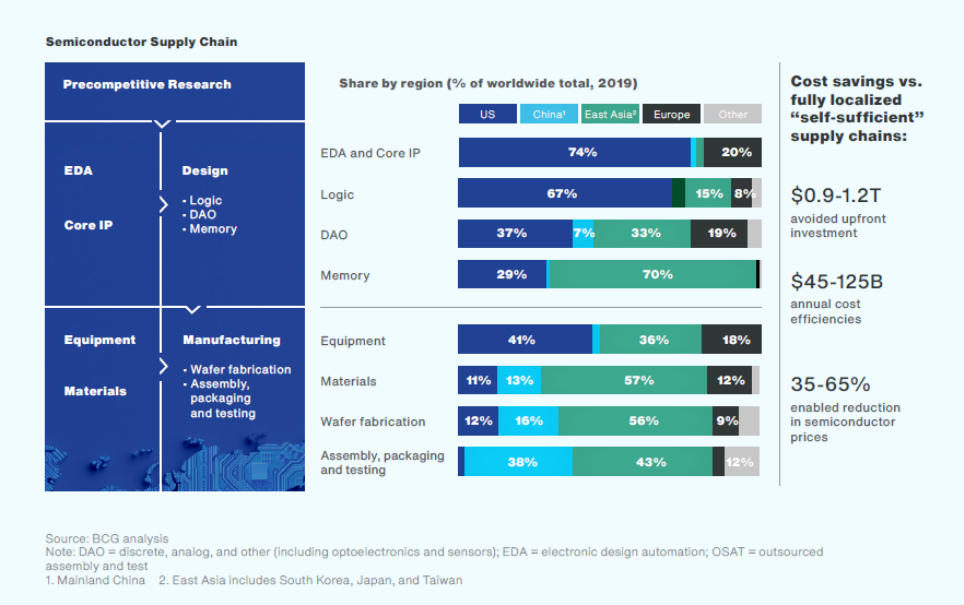
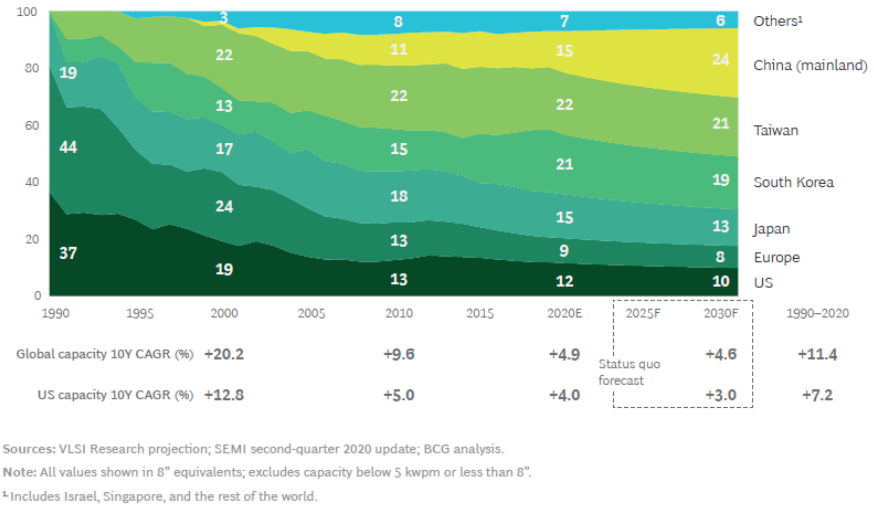


Front-end manufacturing is highly capital intensive due to the scale and complex equipment needed to produce semiconductors. A state-of-the-art semiconductor fab of standard capacity requires roughly $5 billion (for advanced analog fabs) to $20 billion (for advanced logic and memory fabs) of capital expenditure, including land, building, and equipment. This is significantly higher than, for example, the estimated cost of a next-generation aircraft carrier ($13 billion) or a new nuclear power plant ($4 billion to $8 billion)5. Capital expenditure of firms focusing on semiconductor manufacturing typically amounts to 30 to 40% of their annual revenues. As a result, wafer fabrication accounts for approximately 65% of the total industry capital expenditure and 25% of the value added. It is concentrated primarily in East Asia (Taiwan, South Korea and Japan) and mainland China which have been investing heavily to become manufacturing power houses (see figure below).

B – Global manufacturing capacity by location (%)



Sources: VLSI Research projection; SEMI second-quarter 2020 update; BCG analysis.
Note: All values shown in 8" equivalents; excludes capacity below 5 kwpm or less than 8".
¹ Includes Israel, Singapore, and the rest of the world.

Even before the pandemic disrupted the semiconductor supply chain, there was growing political concern in Europe and U.S. about relying so heavily on a small group of Asian suppliers, especially for defense applications and telecommunication networks. With recent chips shortage impacting major industries (automotive, connectivity, etc.), European and U.S. leaders

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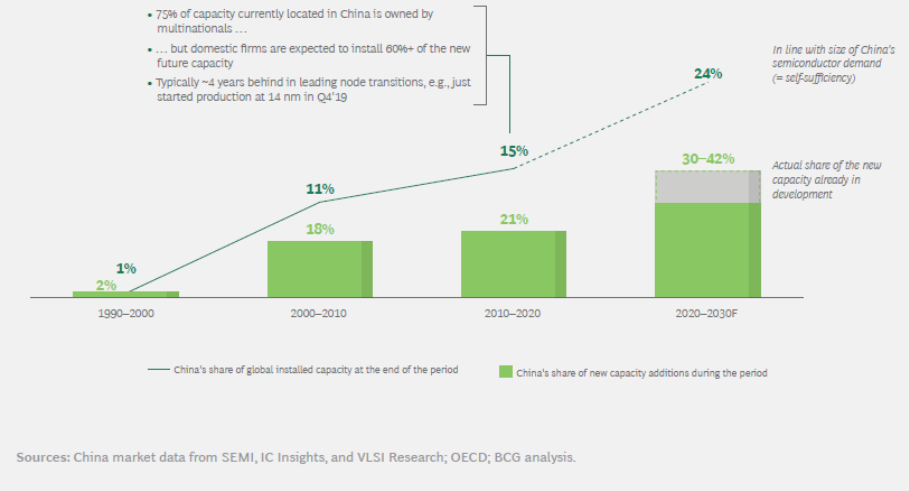
are again calling for "reshoring" of semiconductor chip production for national and economical security reasons. The European Commission, for example, launched in July 2021 an alliance on processors and semiconductor technologies. This translates into two main lines of actions, addressing the main gaps Europe is facing: the reinforcement of the European electronics design ecosystem and the establishment of the necessary manufacturing capacity by a mix of local and global players. Meanwhile a European chips act will be presented in Q1/2022 aimed at building a state-of-the-art European semiconductors ecosystem. In U.S., Biden's administration included $50 Billion in his proposed infrastructure legislation to help the chips industry to build more domestic plants.

China's ambition in semiconductor manufacturing has long been a priority but it gained further urgency with the Made in China 2025 plan and the goal of increasing the semiconductor self-sufficiency. The plan includes investment incentives leading to 30-40% of a new fab's total cost of ownership, equipment acquisition in leasing mode, access to credit and loans at below market rates, etc. However, due to geopolitical tensions, China is facing 2 critical bottlenecks to access to low CMOS nodes manufacturing (<10nm): a study supply of EDA tools and extreme UV lithography equipment.

C – Rapid growth in China's share of the global semiconductor manufacturing capacity



D- Government incentives directly account for 40-70% of US TCO gap

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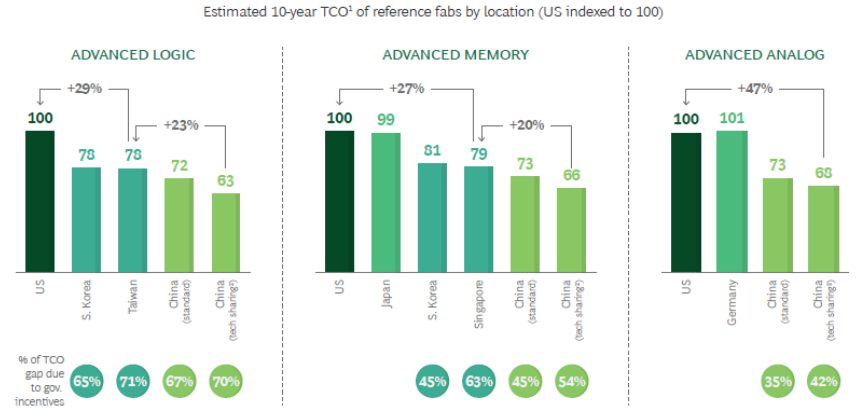

Source: BCG analysis.

[1] TCO includes capital expenditure (upfront land, construction, and equipment) plus ten years of operating expenses (labor, utilities, materials, taxes).

[2] A wider range of incentives, including equipment leaseback with advantageous terms, is available to multinational firms that choose to enter into technology-sharing arrangements in China.

To summarize, in China[15], we see a strong ambition to master semiconductor technology, driven by a self-sufficiency target. This is accelerated by the US/China trade tension. “Big Fund” is the Chinese government’s main vehicle for semiconductor investment and consists of ~50 billion Euro. China has ambition and long-term strategic plans, and is very focused on global merger and acquisition activities, and the investments to make it happen. As an example, ‘’Open Source’’ is an industrial policy tool and important part of its push for technological autonomy for China. In the US a budget of ~50 billion $ for the ‘’Chips for America” program[16] is planned in order to keep the semiconductor industry in the US highly competitive compared to other regions in the world.

[15] https://technode.com/2021/03/04/where-china-is-investing-in-semiconductors-in-charts/ and https://merics.org/en/short-analysis/china-bets-open-source-technologies-boost-domestic-innovation

[16] CHIPS for America Act & FABS Act - Semiconductor Industry Association (semiconductors.org)

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3 Business opportunities & models

The untapped economic potential of next generation wireless network technology for European industry is significant. The driving trends of further densification and increasing network virtualization combined with the opportunity of leveraging new frequency bands in the mm wavelength and the devices required to enable this, is set to trigger a wave of industry driven innovation in Europe. The use of custom wireless networks and accompanying optimalisation of the key parameters for specific business processes (high density of connections, extreme low latency, high bandwidth) which was cost prohibitive prior to the software defined network area now becomes economically viable.

To be the region that seizes these opportunities to the maximum extent, a widespread deployment of the required infrastructure from a shared usage perspective is a key driver of economic growth. To that extent Europe should foster and accelerate the widespread adoption of emerging trends such as Open RAN networks and facilitate both regulatory and financially the shift to network infrastructure as an enabler to deploy new, often software & analytics driven business models. The onset of 5G and the next generation of connectivity technologies brings with it the opportunity to expand the vast economic value driven in the digital world by cloud computing into the physical worlds of business processes. Or in laymen's terms: the next generation of connectivity technologies will give eyes and ears to the cloud and allow the further overlay of digital and all its benefits into the physical processes that drive our private and professional lives. Focusing on open network protocols, standards and infrastructure the same way that standard API's revolutionized interoperability and scalability in software development now also presents a unique opportunity to put Europe at the heart of one connected living lab testbed for next generation network technology where all SME's and smaller players need to help drive the innovation and reap its rewards is a laptop and internet connectivity. Europe also has the right collaborative research models in place at its leading technology enterprises and RTO's to foster this open innovation network. For example, imec's broad portfolio of research collaboration models ranging from shared, precompetitive roadmap driven collaboration between multiple partners across the value chain to dedicated developments on demand provides a solid basis for the ambitions outlined above.

3.1 Large Enterprises

Large enterprises play a crucial role in building up a lead-position in certain areas. The fundaments of a successful value chain are built upon the technological and market leadership of the semiconductor industry. Whereas the European semiconductor industry has this leadership in the automotive value chain, there is potential and room for also taking up a stronger position in the telecom sector. The necessary condition to do so is to create and expand an ecosystem of large enterprises working together throughout the value chain from chip to system on one hand and working together with SME's and RTO's in specific technology competences on the other hand. In the US large enterprises as e.g. Apple and Tesla start developing their own strategic chip-sets. The advantage is that they can own and primary technologies in the products they make and are not dependent on third parties for strategic assets in the value chain. However, whereas originally they had a strong dependency on Intel, they now created a strong dependency on TSMC from a manufacturing perspective. On the

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other hand, the ''Apple-strategy'' does not lead to the best solutions as semiconductor competences are different than system-level competences. Therefore, it is much better to bring together key players in the value chain with their specific competences and build long-term strategic cooperative partnerships to create best-in-class solutions. This also enables partners to specific elements in the system and chip design, such as e.g. energy efficiency, performance, reliability, safety, etc.

COREnect allows the communities of Large Enterprises, SME's and RTO's throughout the value chain to explore each other's key competences, to indicate gaps and needs for the future, translating this into roadmaps, and indicate what each partner can create on its own or through cooperation with others.

One example of a COREnect result is a blog from Ericsson and NXP[17] sharing their views on the importance of joint communication and sensing (JCAS) in 6G networks, reflecting the collaboration between Ericsson and NXP for this to materialize. As this blog is open to others, the idea is also to include other stakeholders in the dialogue and the future joint developments.

Co-creation of new solutions towards different application domains as automotive, communication & connectivity, industry & manufacturing, health & well-being, avionics & space, and others, will become a strategic asset for future successes. In many cases this starts from exploratory projects (e.g. COREnect), leading to larger funded cooperative programs (as covered in a previous section in this document), and resulting in bilateral strategic industrial partnerships between industrial partners (both Large Enterprises as well as SME's) or between industrial partners and RTO's. The most important funded cooperative programs for gaining momentum by large enterprises are IPCEI, KDT and SNS. Programs as HorizonEurope and Eureka (notably via the clusters Xecs, ITEA and CELTIC-Next) enable to focus on particular technology topics on smaller scale.

Systems application industries will greatly benefit from early adoption of 6G services, the 6G roadmap and the cooperation outlined in COREnect. This includes business and differentiation opportunities in new, safe and climate-neutral mobility, advanced, connected manufacturing as well as health services.

One important new element in the business models and business strategy in the future will be the way industries create and make use of RISC-V and Open-Source HW and SW IP. Whereas in the past Large Enterprises only used proprietary IP created by themselves or by third parties, the availability of OpenSource (a.o. RISC-V) will change the way chips are created in the future and partners will work together. This is already common practice in the software world and will

[17] Joint Communication and Sensing in 6G Networks | NXP Semiconductors & Unpacking joint communication and sensing in 6G - Ericsson

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become a reality in the hardware world. A good balance of open-source versus strategic proprietary IP will be fundamental for future chip design and integration into systems.

On the component level further opportunities in future wireless communication arise for semiconductor companies to develop and market new semiconductor processes and devices. Several of those have been outlined in the COREnect roadmap. This includes processors, but also RF-components, power components, sensors based on advanced processes and materials.

Therefore it is key that a dialogue as experienced in COREnect can be continued amongst key stakeholders in a horizontal way (technological competences) as well as in a vertical way (along the value chain in strategic domains for Europe). Thereby it is not needed to have control over the whole value chain, but to have control over a number of strategic assets in the value chain and build industrial relationships on less-critical elements in the value chain.

3.2 SMEs

There is a general perception that opportunities shall arise for SMEs with the deployment of 5G and the advent of 6G. Several reports indicate that "5G will enable SMEs to participate more actively in the communications ecosystem. SMEs will play a particularly crucial role in the success of 5G by contributing to the development of 5G-based applications and technologies that support telecom networks roll-out" and that "there is an opportunity for new European players to enter the [5G] market, [as] diversification is paramount to European and American operators". A public consultation launched by COREnect highlighted the opportunity for SMEs to target a particular part of the technology or of the market value chain, validate forward-looking innovative advanced products, and cooperate with academic institutions for the implementation of technology at early stage.

Main challenges to overcome for SMEs include dependence on large scale trial / pre-commercial infrastructures to test SME products; heavy investment required to contribute to standardisation, and in relation with IPR and patent-related issues; and the fact that the EU telecoms market is (still) fragmented, making it very challenging for SMEs to broaden their market within the EU.

In terms of R&D, SMEs benefit from all initiatives mentioned in section 2.3 all welcome SMEs, to varying degree. Still, dedicating specific envelopes within Horizon Europe for SMEs working on components for future connectivity systems, e.g., via a joint effort between the SNS and KDT JUs, could prove worthwhile. Likewise, the flexibility of the Eureka Clusters, where SME participation is traditionally significant (e.g., around 40% for the PENTA programme), could be put to good use to encourage R&D collaborative projects grouping ECS and telecommunications actors with strong SME involvement.

Other investment measures more dedicated to SMEs focus on the issue of bridging the gap between R&D and the market take-up. Such initiatives as InvestEU, supported jointly by the EC and the EIB, as well as the instruments from the EIC, are mostly dedicated to such investment. Private initiatives should also be encouraged. Such initiatives could include:

- Encourage corporate participation in targeted investments in VC funds that finance early-stage SMEs developing advanced connectivity applications. Both microelectronics and telecoms corporates should be involved (in telecoms: both equipment

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manufacturers and telcos), as well as vertical corporates benefiting from European-based components and systems (e.g., automotive, manufacturing).

- Create a dedicated co-investment platform focusing on components for 6G, again involving corporate VCs from microelectronics, telecoms, and verticals.
- Create pan-European sandboxes, a one-stop shop where a company would apply for approval and would be automatically eligible to offer products and services throughout the EU market.

Another important area where investment should be strengthened to support innovative SMEs lies in the benchmarking and trialing of the products and solutions, as highlighted by COREnect's Expert Group 2.

3.3 RTOs

The vital role that European RTOs and their industry-driven research programs can play in bridging the role between academic research and industry validation will be an essential part of successfully implementing the vision outlined above. Creating a common basis of pre-competitive technology building blocks that can feed a broad set of connectivity applications in various fields is essential for the growth of the ecosystem as a whole and by definition transcends the R&D ambitions of individual companies. These types of programs also form the basis of a broad talent pool through the influx of PhD students that supports the sustainable growth of the sector, which is essential in the ever-increasing global war for technology talent to nurture the next generation of EU technology leaders.

Furthermore, the past has already proven that the research programs of the RTOs are the cradle for many spin-offs. A considerable amount of spin-offs created from RTOs operate in the field of connectivity and given the fact that the RTOs in Europe are very active in the field of connectivity, more spin-off initiatives are expected to arise from RTOs in the field of connectivity.

Transfer of research and know-how from RTOs is also happening to large companies in the form of common participation of funded projects, participation of companies to reseacrh programs of RTOs as well as bilateral collaborations. In the field of connectivity, such transfers will be needed, for example in the domains of semiconductor, packaging and heterogeneous integration technologies. Such transfers come on top of the transfer of talent in these domains.

The various engagement models also play an essential role in facilitating access to state-of-the-art technology available today for SMEs, start-ups and academia through lowering the threshold to engage in technology development by various forms of bundling projects in MPW setups or providing easy access to design and prototyping services. One example of this is the successful EUROPRACTICE model which covers a broad range of s technologies (mainly semiconductor technologies) that are needed in connectivity applications. Other types of services could be in the form of services through test beds, making measurement infrastructure available to SMEs and other interested stakeholders.

Finally, the shared insights of the RTO community also play an invaluable role in policy formation by acting as a sounding board and advising in a broad range of European forums on standardization and regulation of emerging connectivity technologies.

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4 High-level recommendations to build a stronger sovereign position of Europe towards a flourishing 6G microelectronics industry

4.1 General recommendations

Europe has the potential to build a strong sovereign position in the area of 5/6G-related microelectronics industry, similar to the current position in the automotive industry. To do so, several recommendations have been formulated below.

It is important to create and strengthen concrete actions for market growth through technological excellence to build economic sustainable sovereignty and resilience.

It is mandatory to ensure a level playing field of Europe with the rest of the world, as well as within Europe amongst the Member States. Public and private investments in Europe need to be equal to what is happening in the rest of the world to stay competitive and grow or keep market leadership.

In contrast to some opinions stating that Europe should build up or regain sovereignty in all areas of the value chain, COREnect believes that it is more important to have control over several critical and/or strategic parts of the value chains. It is also recommended to build up value networks rather than value chains, as there is more and more cooperation on horizontal levels throughout different value chains.

Furthermore, strategic priorities between Europe, Member States and Industry need to be further streamlined, especially forthe definition of top-priority ambitions. The SRIA's from KDT and SNS are good ways to define future roadmaps and priority topics for research and innovation. The IPCEI2 program on Microelectronics and Communication Technologies is an ideal platform to realize enough momentum and critical mass to achieve excellent results and translate longer term technological ambitions into market success.

Eco-systems of large enterprises, SME's and RTO's need to be further enhanced, both in horizontal competence areas as well as in vertical value chains. Joint strategic developments are needed amongst semiconductor companies (e.g. "Airbus of RISC-V") and between OEMs & semiconductor companies (e.g. joint common domain-specific processor & platform developments)

Within European and national cooperation programs, "Fast-Track initiatives"' should be set up for smaller-scale key advancements in specific technological areas.

In general, the European cooperative funding programs are working well in many aspects. It truly generates pan-European cooperation and has enabled the set-up of long-living eco-systems in different horizontal technology and vertical application domains, consisting of large industries, SME's, RTO's and universities. Furthermore, different types of programs enable to cover almost the complete TRL-chain. Many projects have yielded excellent results, both from a microelectronics as from a communication and connectivity perspectives.

However, attention should be paid to further improve the efficiency of the process and administration for this type of projects, as mentioned hereunder.

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The time between proposal submission and start-of-the-project is still too long for most of the programs. In a number of cases it takes almost one year, which is very long from an industrial perspective. For IPCEI it takes even more than 2 years between start of proposal writing and approval.

There is an uncertainty in financial support for some instruments, especially the commitment from different member states in KDT and in EUREKA is often lacking or remains unclear for a too long time.

Furthermore, the priority of technical expert proposal evaluations versus national economic strategic preferences is often unclear, especially in the Eureka framework.

The administrative overhead in most schemes is too high, especially in KDT and HorizonEurope.

Some programmes consist of relatively small focused technology projects (e.g., Horizon Europe), while other programs focus on very large consortia (e.g., KDT), where all partners have a relatively smaller contribution. There should also be large strategic projects with only a limited number of partners, who are either key players in Europe or partners bringing potential disruption and innovation, to ensure or future market leadership in particular domains. Such "flagship projects" are already present in the 5G PPP and are planned in the SNS Partnership, and have been happening in CELTIC-NEXT for many years.

At first sight, there shall be an increase of top-down topics in KDT. Taking into account the strategic nature of connectivity, and especially 6G, one could recommend to make one or more dedicated calls on 6G with all involved key stakeholders in Europe within the KDT and the SNS frameworks.

4.2 Specific recommendations related to SMEs

When it comes to SMEs, COREnect's recommendations fall into three categories:

4.2.1 Recommendations promoting the role of SMEs in the ecosystem(s)

- Strengthen the interaction between corporate companies, research organisations, and SMEs. The main objective is to gather the best researchers in the field and ensure that Europe will be at the edge of components for 6G.
- Enable matchmaking between European SMEs, and with other European stakeholders. This should cover technology, innovation, education, finance, and funding. It shall be oriented not only towards start-ups, but also towards spin-offs and established SMEs. The main objective is to overcome the issue of Europe not succeeding in creating companies worth hundreds of billions of euros (like what is being achieved in the US and China).
- Focus on existing European strengths, e.g., industrial applications.

In other words the recommendation is to create a European ecosystem where close collaboration between stakeholders from the microelectronics and connectivity domains will be possible. This shall allow Europe to compete at global level. To achieve this, it would be beneficial if one or more European champion(s) from these domains could "lead the way".

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4.2.2 Recommendations only for SMEs

- Dedicate specific envelopes within Horizon Europe for SMEs working on components for future connectivity systems, e.g., via a coordinated effort between the SNS and KDT Partnerships. An alternate (or complementary) option would be to set a KPI for SME participation in / contribution to a given instrument. As a (good) example, the SNS JU expects a minimum of 20% participation from SMEs[18]. During the 3rd COREnect workshop[19], EC representatives stressed that they were looking at increasing the SME participation in the KDT JU, with respect to the participation reached in the previous ECSEL initiative. Indeed, indicating clearly a KPI for SME participation seems to be a good trigger to increase SME participation, as demonstrated in the 5G Public-Private Partnership, where 22% SME participation was reached (in budget).
- Encourage corporate participation in targeted investments in VC funds that finance early-stage SMEs developing advanced connectivity applications. Both microelectronics and telecoms corporates should be involved (in telecoms: both equipment manufacturers and telcos), as well as vertical corporates benefiting from European-based components and systems (e.g., automotive, manufacturing).
- Provide more support to SMEs facing heavy investment after the first patent is filed and/or the first solution is being developed.
- Create a dedicated co-investment platform focusing on components for 6G, again involving corporate VCs from microelectronics, telecoms, and verticals.
- Create pan-European sandboxes, a one-stop shop where a company would apply for approval and would be automatically eligible to offer products and services throughout the EU market.

4.2.3 General recommendations applicable to SMEs

- Support an EU open-source computing hardware ecosystem, to lower the entry costs for new chip designs.
- Spread innovation beyond Horizon Europe. “Innovation should be spread across the entire EU framework of regional policy, agriculture, and structural funds”, says MEP Maria da Graca Carvalho.

Instruments of the EIC as well as InvestEU are positioned to support SMEs that are closer to the market than programmes such as KDT, SNS, Xecs, Celtic-Next, or IPCEI. Although SMEs are encouraged to contribute to those R&I programmes, the effort involved in the preparation of proposals is often heavy and not specifically adapted to SMEs -especially for IPCEI. Eurostars might prove to be a instrument more suited to SME needs, but it does not address market take-up. The 3rd COREnect workshop highlighted that one of the key components for success will be to use a “range of policy instruments that will be available to achieve the common goals”.

[18] "One of the SNS Programme KPIs is the participation of SMEs at the RIA and IA activities at a level of 20%", SNS R&I Work Programme 2021-2022, Smart Networks and Services Joint Undertaking.

[19] Cf. https://www.corenect.eu/workshops/blog-post-title-three-jbnab.

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4.3 European 'champion(s)'

One of COREnect's objectives is to "create the conditions for one or more European champion(s) in the domain of core technology for attaining technology sovereignty in future connectivity systems". COREnect believes that there is room in the next 10 years for the emergence of European champions in the combined domains of microelectronics and connectivity.

4.3.1 Conditions for an EU champion in the field

What are the conditions for an EU champion in the field? Do we need to "think differently", and look at game changer companies like Tesla as an example? Or to launch a new Airbus-type strategic initiative? COREnect recommends to primarily be pragmatic: come up with a common goal that is easily comprehensible, and then "rally the troops", i.e., build the ecosystem to achieve this goal. The simple vision / goal would facilitate setting up such an ecosystem collaboration, and the corresponding support. Such a strategic decision could come either from industry or be a political decision at EU level -or a combination of both. This would lead to a top-down approach -formulating a clear goal and then put the means to achieve this goal.

However, innovation often comes in a bottom-up manner. Disruptive ideas are likely to be there already, in SMEs as well as in large companies and in academic institutions. We need to make all the best effort in Europe to lower the barrier for growth and support to make those ideas strive. To achieve this, COREnect recommends in addition to the recommendations made in section 3.2.1, to focus on strengthening support for more cooperation among EU companies. For example, technological SMEs could benefit from large connectivity players (Nokia, Ericsson) indicating their microelectronics-related requirements in advance. Too often, such players just rely on / pick up the latest available products. A partnership between those large companies and SMEs to work in advance on future requirements could be established, for the benefit of both SMEs and large companies.

4.3.2 Technological domains to be addressed

COREnect does not recommend prioritising a specific domain where champions would emerge, considering that innovation and disruption often comes where it is not expected. Still, and although forecasting in innovative and disruptive technologies is challenging, it looks like if such a European champion were to emerge, there is a distinct possibility that it might be in semiconductor design. This idea is shared by COREnect's Expert Groups, who recommends in the short term to "ease access to advanced silicon technologies, design tools, license and IP in order to strengthen SOC design competency in EU", in the medium term, to "Increase IC design capabilities in advanced logic technologies", and in the long term to "create incentives to attract and educate sufficient engineers students to end-to-end system design programs (from low-level analogue IC design up to high-level application software)"[20]. This also seems to be the

[20] COREnect Deliverable 3.7 "Core Technologies Development Recommendations and Guidelines", section 2.2 "infrastructure connectivity". There are similar recommendations for automotive grade connectivity, industry grade connectivity, and consumer grade connectivity.

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opinion of ASML, which states in their "EU Chips Act Position Paper" that a roadmap should "maximize the potential of European champions in semiconductor design, manufacturing equipment and materials, on which the global semiconductor ecosystem depends"[21]. In order to facilitate the emergence of such a champion, COREnect recommends helping SMEs access silicon manufacturing design facilities from research institutions.

There are also plenty of niche applications for SMEs specialising in photonics. Novel ideas, e.g., when combining chips together, might prove effective to create conditions for some European SMEs to strive.

4.3.3 Start-up, spin-offs, JV, or else?

COREnect does not make any assumption as to what form such champions would take: start-ups, spin-offs, Joint Ventures… The recommendations in the previous sub-sections are primarily focusing towards SMEs and the potential creation of start-ups and spin-offs as potential champions. Let's consider now the option of a formal partnership / collaboration between two (or more) large companies, e.g., a Joint Venture (JV)[22].

Such JVs in the microelectronics and connectivity domains have already happened in Europe. A specific example that comes to mind is the ST-Ericsson Joint Venture that happened in the 2010's, resulting from the merger of four companies issued from branches from Ericsson, ST, as well as a former NXP acquired company. Other examples, this time between a European company and a non-EU company, include Sony-Ericsson in the 2000's, and Ericsson-GE in the 1990's. While such Joint Ventures were not always a success from a business point of view, lessons can be learned for the future.

It is interesting to note that all those JVs were initiated by the private side, without any public intervention. In all cases, it happened because at one point in time business plans were aligned on both sides, and there was a nice fit in terms of complementary activities, allowing both parties to strengthen and expand on a given market, i.e., mobile phones for consumers in the case of Sony-Ericsson, and wireless-oriented chips for ST-Ericsson.

What could trigger such a partnership to be initiated in the first place? If we refer to the above-mentioned examples, a few factors were critical:

- An alignment between the plans of the companies involved, e.g., looking at expanding their markets in the same direction;
- Complementary activities that could lead to solving current challenges and strengthening the competitivity of each of the parties, e.g., via the expansion of the current portfolio of products and solutions;
- Complementary expertise, i.e., missing expertise in one company that could be brought by the other party;
- Investment and risk too high for one company to pursue it on its own;

[21] "EU Chips Act Position Paper". February 2022, ASML.

[22] The partnership/collaboration could also be between one or more large companies and one or more SMEs.

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- An already existing (supplier-vendor) cooperation that had established a certain level of trust between the parties;
- A few individuals in each of the companies willing to lead the partnership.

There are however challenges when creating such ambitious partnerships, in particular:

- Creating a common strategy and roadmap for the new partnership;
- Establishing a streamlined portfolio of products and solutions;
- Selecting leadership with the required competence and freedom of bias;
- Establishing values and culture relevant for the new business scope;
- Selection of infrastructure and tools used across the new, consolidated organization.

To prevent those challenges from disrupting a potential success, here are a couple of recommendations:

- Establish a clear strategy and decision process before the formal start of the partnership;
- Prioritize market competitiveness and customer needs when defining the new portfolio;
- Make legacy overlaps in the new portfolio short-lived or, better, non-existent;
- Make domain expertise and absence of bias a priority in leadership recruitment;
- Identify and recognize the needs of the changed business scope in terms of policies, values, and culture.

The microelectronics domain has recently become a major centre of strategic attention in Europe, leading to the initiation of a “Chips Act”. This is without a doubt one of the major outcomes of Europe’s recent effort to strengthen its technological sovereignty. Although the previous JVs listed above were 100% decided by private organisations, it is COREnect’s belief that the current context is more favourable to a more stringent cooperation between the public and private sides, if such a partnership towards the creation of one of more European champions were to be initiated in Europe in the near future.

But what about microelectronics for connectivity? In the 2000’s, telecommunication was a high priority market for microelectronics companies, who responded swiftly to any requests from telecom manufacturers for new chips. However, with the explosion of consumer electronics, this market has decreased in importance since then. Still, the telecoms market is important from a technological perspective, as it keeps pushing the technology envelope very aggressively. Thus, connectivity can still be considered as quite important for the microelectronics sector, and probably have more leverage than its share of the total market would imply.

Other challenges facing the development of a strong microelectronics for connectivity sector in Europe lie with the following:

- It is difficult to find the right talents in semiconductor design. There is not enough research in this domain, and students who are involved in the domain are often not in the EU;
- Cutting edge CMOS is not in Europe.

Indeed, one of the current challenges is that telecommunications manufacturers tend to turn more to suppliers outside the EU, such as Intel or Samsung, because such companies are more at the edge with respect to their needs than EU companies are at the moment. This is somewhat reflected in the Intel announcement of the first phase of an investment which could reach €80

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billion in Europe[23], and which was hailed by the European Commission as the first sign of success for its Chips Act. The solution to this might be either to reinforce the capacity of the European microelectronics sector to respond to those challenging needs, or to strengthen the in-house capabilities of telecommunications manufacturers in terms of chips design -the latter being already in progress.

[23] "EU hails €80 billion Intel investment as first success for Chips Act", 17 Mar 2022 | The US chipmaker has announced billions for new foundries and R&D hubs across the continent, https://sciencebusiness.net/news/eu-hails-eu80-billion-intel-investment-first-success-chips-act

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5 Conclusion

The European Commission's proposal for a European Chips Act (the "Chips Act") aims to more than double Europe's share in global semiconductor production capacity to 20% by 2030. This is a very ambitious goal – some might even say unrealistic – but without healthy ambition, there can be no progress. However, Europe should not only focus on increasing Europe's chip production capacity or getting the most advanced manufacturing nodes in Europe. It should aim to double Europe's relevance in the global semiconductor industry. Enhancing EU's capabilities in chip design is a key building block of a sustainable and impactful EU chip strategy.

IP and chip development for the EU key verticals Automotive, Industrial, 6G, Health, Smart Home must be a priority area for Europe. This will not only strengthen the European semiconductor sector but also the ability of EU's lead industries to develop cutting-edge products ahead of global competition. A main objective shall be to launch targeted programs aiming at bringing industry (large and small), RTOs and universities together, to create IP and chip solutions with a clear commercialization roadmap. A balance between academic and industrial research and development funding should be ensured, to leverage the innovation potential as effectively as possible. A good mix of specialized smaller scale funding programs and initiatives as IPCEI with enough critical mass to create a momentum for technology leadership and market success for longer term ambitions in semiconductor industry and the vertical value chains. The funding instruments should be as agile as possible and fit-for purpose, given the dynamic market developments. Innovations in digital as well as analogue/mixed signal ICs should be in the scope of any future and existing program. Europe needs both angles to secure a leadership position at global scale. Especially for the green transformation of the economy, industry will heavily rely on a combination of analogue (e.g., battery management) and digital (e.g., edge computing) chips - complemented with advanced packaging innovations. Being as independent as possible on key IP for these crucial applications must be the goal. Another important focus area is the development of chips with open-source hardware and software, including the use of the RISC-V processor architecture as a field of action. This is a vital element of building a resilient EU chip ecosystem. Creating IP cores "made in Europe" is required to be more independent in the future, especially given geopolitical and economic uncertainties.

Automotive, industrial electronics and wired and wireless infrastructure are strategic European industries with strong competitive positions on a global scale. These industries are increasingly dependent on semiconductor technology, with double-digit growth rates. Investments in the European semiconductor ecosystem will strengthen the global competitiveness of these European industries, through a front-row position and/or easier access to semiconductor technology.

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6 Annex : Comparison between COREnect priorities and ECS SRIA content

6.1 ECS SRIA content related to materials, device and packaging technologies echoing COREnect priorities

These priorities are developed in two SRIA foundational technology chapters:

- Chapter “Process Technology, Equipment, Materials and Manufacturing”
    - This chapter stresses the importance of new computing architecture paradigms such as near-memory or in-memory computing and neuromorphic computing, that strongly reduce the movement of data, and accordingly allow decreased overall energy consumption. It states that specific low-power transistors, memory and 3D-integration technologies need to be developed to ensure close coupling between computer and memory blocks. This idea is echoed in the cross-sectional technology chapter “Edge Computing and Embedded Artificial Intelligence”;
    - Major Challenge 1 “Advanced computing, memory and in-memory computing concepts” mentions that advanced 3D and optical input/output (I/O) technological solutions to circumvent limitations of traditional I/O’s architectures are strengths to foster and build upon in Europe. It also stresses the need to develop new embedded non-volatile memory (eNVM) technologies to enable local AI processing and storage of configuration data.
    - Major Challenge 2, “Novel devices and circuits that enable advanced functionality”, identifies research needs on materials for energy harvesting, micro-batteries, supercapacitors and wireless power transfer. It also calls for research on advanced RF and photonics communication technologies to interface between semiconductors components, subsystems and systems, stating that these technologies should enable better and more energy-efficient control of emission and reception channels (for example, for 5G connectivity and 6G preparations) via:
        - New energy-efficient RF and mm-wave integrated device options, including radar (building on e.g. SiGe/BiCMOS, FD SOI, CMOS, PIC).
        - Energy-efficient computing and communication, including a focus on developing new technologies,
        - Bringing MOEMS and micro-optics, nanophotonics, optical interconnections, photonics-enabled device and system options into a CMOS-compatible manufacturing and/or packaging flow.
        - Integration of solid-state light emitters such as LED and laser with, or onto, a CMOS-compatible platform.
    - Finally, Major Challenge 3 “Advanced heterogeneous integration and packaging solutions” of that SRIA chapter cites the following advanced interconnect, encapsulation and packaging technologies:
        - Specific power and RF application technologies

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        - Solutions for high-frequency miniaturisation, such as for mm-wave applications (> 60 GHz) and for > 100 GHz towards THz applications for which no package solutions currently exist.
- Chapter “Components, Modules and Systems Integration”
    - In that chapter, Major Challenge 1, “Physical and functional integration”, mentions communications as one of its key focus research areas, with the aim to
        - Module-level high-speed communication features, including current and new frequency bands.
        - New front-end components, filters and functionalities e.g. active antennas for 5G and 6G communications and non-terrestrial network solutions
        - Low latency and low power communications in-package/module as well as at system level for the edge and IoT devices.
        - Strategies and components for Electromagnetic interference (EMI) mitigation.
        - High-performance signal quality in harsh environmental conditions
    - Energy and thermal management is another focus area, notably with the need to develop solutions for thermal management for integrated photonics
    - Major Challenge 2, “Materials for integration”, calls for research on functional materials for integrated photonics, for efficient modulation, higher bandwidth, modulation/detection, and for functional components at frequencies above 10 GHz: CMOS or GaN-compatible thin film piezoelectric materials, materials for high-efficiency acoustic transduction.
    - Finally, in that chapter, Major Challenge 3, “Technologies, manufacturing and integration processes”, identifies as key research topics:
        - Photonic system integration based on silicon photonics (and other substrates), multi-domain integration to photonic systems, including RF, MEMS/NEMS, sensors, etc.; electro-optic co-packaging.
        - Enabling electronic-photonic systems by heterogeneous integration (III-V, ferroelectrics, ultra-low-loss waveguide materials).
        - Heterogeneous integration processes and equipment for integrated photonics, including high-precision component placement and bonding, as well as low-loss fiber coupling.

6.2 Consolidation of priorities from expert groups & link with ECS SRIA

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Short term (<2026) EG priorities	2022 ECS SRIA priorities
Improve existing European eNVM (CS)	Part of Major challenge 1 of Chapter 1.1 : Advanced computing, memory and in-memory computing concepts. "New embedded non-volatile memory (eNVM) technologies to enable local AI processing and storage of configuration data"
Development of open modular microkernel-based OS (CS)	Not discussed in ECS SRIA
RIA projects on telecom applications operating in the W-band (75-110 GHz) and D-band (CC/CI/RAN)	Ch 1.2, MC 1, topic 1.3 "High-speed 5G and beyond 5G connectivity"
High-frequency, thermally efficient packaging substrate technologies with embedded antenna array elements (CC/CI/RAN)	Ch 1.1, MC3: "Solutions for high-frequency miniaturisation, such as for mm-wave applications (> 60 GHz) and for > 100 GHz towards THz applications for which no package solutions currently exist" Ch 2.2, MC1, "Innovative packaging and PCB technology targeting connectivity application" Ch 2.2, MC2: "subTHz connectivity application in the 200 GHz – 300 GHz band:"
Research on integrating InP and GaN devices on silicon (CC/CI/RAN, CC/CG)	Ch 2.2, MC 1 From LTV chapter, section "Process technology, equipment, materials and manufacturing": "Millimetre-wave front-ends with III-V MOSFETs have to be developed (with applications in communications, radar, etc), including 3D aspects of processing"
Research on efficient testing of mm-wave and sub-THz circuits (CC/CI/RAN)	Not discussed in ECS SRIA
Developing <28nm FDSOI and SiGe HBT with fT, fMAX > 600GHz (CC/CI/RAN, CC/CG)	Ch 1.1, MC2, "New energy-efficient RF and mm-wave integrated device options, including radar (building on e.g. SiGe/BiCMOS, FD SOI,…)" Ch 2.2, MC1, "Innovative differentiated semiconductor technology development targeting connectivity application.". Lists RF SOI and FD SOI
Establish components (photonic and electronics) for optical transceivers with baud rates 100…130Gbaud: modulators and detectors with bandwidths of at least 80GHz; front-end driver and receiver electronics with analog bandwidths between 60GHz to 90GHz; analog-to-digital and digital-to-analog convertors integrated using scaled CMOS with sampling rates >>100GS/s, analog bandwidths >50GHz and 5-6bit ENOB (CC/CI/WI)	Ch 1.1, MC1: "The option to use advanced 3D and optical input/output (I/O) technological solutions to circumvent limitations of traditional I/O's architectures are strengths to foster and build upon in Europe." Ch 1.1, MC 2 "Advanced RF and photonics communication technologies to interface between semiconductors components, subsystems and systems"
Establish components (photonics and electronics) with ultra high channel counts (100s of channels), integration density (>>100Gb/s/mm), and energy efficiency (< 1pJ/bit) for co-packaged optical interfaces on new generations of switch ASICs, GPU's, CPU's. (CC/CI/WI)	Not discussed in ECS SRIA

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2.5D/3D heterogeneous integration for UE equipment operating at mm-wave and sub-THz (CC/CG)	Ch 1.1, MC2 "Bringing MOEMS and micro-optics, nanophotonics, optical interconnections, photonics-enabled device and system options into a CMOS-compatible manufacturing and/or packaging flow; Integration of solid-state light emitters such as LED and laser with, or onto, a CMOS-compatible platform" Ch 2.2, MC1: "Enable a European ecosystem that can support heterogeneous integration (multi-die system in a package, advanced assembly capability, advanced substrate manufacturing, etc) to help European players capture higher value in the connectivity market." Long term vision chapter, subsection "Components, modules and systems integration": "closer integration of electronics and photonics with PICs and fast semiconductor driving/control/sensor components"
Research on joint communication and sensing (CC/CG)	Not discussed in ECS SRIA
RIA projects targeting industry grade communication systems and solutions (CC/IG)	Not discussed in ECS SRIA
Develop AI cores for edge sensors	Ch 2.2, MC2: evaluation of the AI concept to handle the complexity of future connectivity networks (for example, 6G), and to improve efficiency and adaptability
Research on Si batteries, integrated batteries, energy harvesting technologies, micro solar panels (SP/IG)	Ch 1.1, MC2: "Materials for energy harvesting (e.g. perovskite solar cells, piezoelectric ceramics and thin films) and storage (e.g. perovskites, ferroelectrics and relaxors), micro-batteries, supercapacitors and wireless power transfer"

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Medium term (2026-2030) EG priorities	2022 ECS SRIA priorities
Invest in 2.5D and 3D packaging (CS)	Ch 1.1, MC 3: "Advanced packaging technologies are required for mm-wave applications (> 30 GHz), both GaN/Si RF and high-electron-mobility-transistor (HEMT) devices"
Transition from the classic memory hierarchy used in von Neumann computers to memory used in emerging non-von-Neumann computers (CS)	Chapter 2.1 "Edge computing and embedded artificial intelligence" Chapter 2.3 "Architecture and design: methods and tools" MC3 "managing complexity", "architectures and tools for non von-Neumann and neuromorphic computing"
RIA projects on telecom applications operating in the W-band (75-110 GHz) and D-band (CC/CI/RAN)	Not discussed in ECS SRIA
Heterogeneous integration technology R&D (CC/CI/RAN)	Ch 2.2, MC1: "Enable a European ecosystem that can support heterogeneous integration (multi-die system in a package, advanced assembly capability, advanced substrate manufacturing, etc) to help European players capture higher value in the connectivity market."
Grow ecosystem around InP, including co-integration with silicon (CC/CI/RAN)	Ch 2.2, MC 1
Process technologies for photonics that allow E/O and O/E conversion bandwidths beyond 100GHz (CC/CI/WI)	Ch 1.1, MC1: "The option to use advanced 3D and optical input/output (I/O) technological solutions to circumvent limitations of traditional I/O's architectures are strengths to foster and build upon in Europe." Ch 1.1, MC 2 "Advanced RF and photonics communication technologies to interface between semiconductors components, subsystems and systems" Discussed, but could be developed
Deploy IC technologies (SiGe BiCMOS, InP) that allow integration of functionality with bandwidths far beyond 100GHz (CC/CI/WI)	Ch 2.2, MC2: "European activity in the spectrum > 300 GHz should be encouraged" From LTV chapter, section "Process technology, equipment, materials and manufacturing": "Millimetre-wave front-ends with III-V MOSFETs have to be developed (with applications in communications, radar, etc), including 3D aspects of processing"
Integration approaches for photonics and electronics that allow a dense integration of a large amount of connections with bandwidths in excess of 100GHz (MCM, 3D) (CC/CI/WI)	Ch 1.1, MC2: "By leveraging mature semiconductor manufacturing methods, engineered wafers that incorporate SOI technology offer a powerful approach toward broader adoption of advanced chip-scale integrated optics"
novel optical transceiver architectures, where functionality is shifted further into the optical domain: optical-domain equalization, optical-domain interleaving (CC/CI/WI)	Not discussed in ECS SRIA
Further research on HF communication (SP/IG)	Not discussed in ECS SRIA
Alternative solutions for power distribution (SP/IG)	Not discussed in ECS SRIA
Further research on optical communication (SP/IG)	Not discussed in ECS SRIA

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Expand radar sensing in higher frequencies (SiGe leads the way, CMOS needs to follow) (SP/AC)	Ch 1.1, MC2: "Advanced RF and photonics communication technologies to interface between semiconductors components, subsystems and systems: These technologies should enable better and more energy-efficient control of emission and reception channels (for example, for 5G connectivity and 6G preparations) via: New energy-efficient RF and mm-wave integrated device options, including radar (building on e.g. SiGe/BiCMOS, FD SOI, CMOS, PIC)"
Long term (>2030) EG priorities	**2022 ECS SRIA priorities**
Address research questions related to eNVM improvements (CS)	Part of Major challenge 1 of Chapter 1.1 : Advanced computing, memory and in-memory computing concepts. "New embedded non-volatile memory (eNVM) technologies to enable local AI processing and storage of configuration data" From LTV chapter, section "Process technology, equipment, materials and manufacturing": "In the field of alternative memories, resistive RAM, magnetic RAM and ferroelectric RAM/FeFET will be key for driving the limits of integration and performance beyond that afforded by existing non-volatile, DRAM and SRAM memories"
Optoelectronic based mm-wave and sub-THz generation and processing by heterogeneous integration with photonics technologies (silicon photonics and III-V-based) (CC/CI/RAN)	Ch 2.1, MC3: "Technologies, manufacturing and integration processes • Photonic system integration based on silicon photonics (and other substrates), multi-domain integration to photonic systems, including RF, MEMS/NEMS, sensors, etc.; electro-optic co-packaging. • Enabling electronic-photonic systems by heterogeneous integration (III-V, ferroelectrics, ultra-low-loss waveguide materials). • Heterogeneous integration processes and equipment for integrated photonics, including high-precision component placement and bonding, as well as low-loss fiber coupling."
Further research on power over fiber (SP/IG)	Not discussed in ECS SRIA
Highly integrated THz imaging (SP/AC)	Development of imaging technologies across many frequency domains is discussed in several chapters of the ECS SRIA

Abbreviations:

For the EG priorities column:

- CS: Compute and storage (EG1)
- CC/CI/RAN: Connect and communication (EG2) / Connectivity Infrastructure / RAN
- CC/CI/WI: Connect and communication (EG2) / Connectivity Infrastructure / Wired infrastructure
- CC/CG: Connect and communication (EG2) / Consumer grade Connectivity
- CC/IG: Connect and communication (EG2) / Industrial grade Connectivity
- SP/IG: Sense and Power (EG3) / Industrial grade Connectivity
- SP/AC: Sense and Power (EG3) / Automotive Connectivity

For the ECS SRIA column: MC = Major Challenge

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